SSD1309

Advance Information

128 x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

Appendix: IC Revision history of SSD1309 Specification

Version	Change Items	Effective Date
0.10	1st Release	12-Oct-10
1.0	1. Changed to Advance Information 2. Add SSD1309UR1 in ordering information. (P.11 , P.55)	14-Oct-10
1.1	1. Added Command 26h/27h/29h/2Ah/2Eh/2Fh/A3h/DCh in Section 9 & Section 10 (P.28~31, P.33, P.45~48) 2. Revised default value of A[7:4] of command D5h in Table 9-5 from 1000b into 0111b. (P.34)	25-Jul-11

CONTENT

FIGURES

TABLE

1 GENERAL DESCRIPTION

SSD1309 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64 commons. This IC is designed for Common Cathode type OLED panel.

The SSD1309 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. It has 256-step brightness control. Data/Commands are sent from general MCU through the hardware selectable 6800/8080 series compatible Parallel Interface, I^2C interface or Serial Peripheral Interface. It is suitable for many compact portable applications, such as mobile phone sub-display, MP3 player and calculator, etc.

2 FEATURES

- Resolution: 128 x 64 dot matrix panel
- Power supply
  - V_{DD} = 1.65V ~ 3.3V for IC logic
  - V_{CC} = 7.0V ~ 16.0V for Panel driving
- For matrix display
  - OLED driving output voltage, 16V maximum
  - Segment maximum source current: 320uA
  - Common maximum sink current: 40mA
  - 256 step contrast brightness current control
- Embedded 128 x 64 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8-bit 6800/8080-series parallel interface
  - 3 /4 wire Serial Peripheral Interface
  - I^2C Interface
- Screen saving infinite content scrolling function
- Programmable Frame Rate
- Programmable Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- On-Chip Oscillator
- Chip layout for COG , COF
- Wide range of operating temperature: -40°C to 85°C

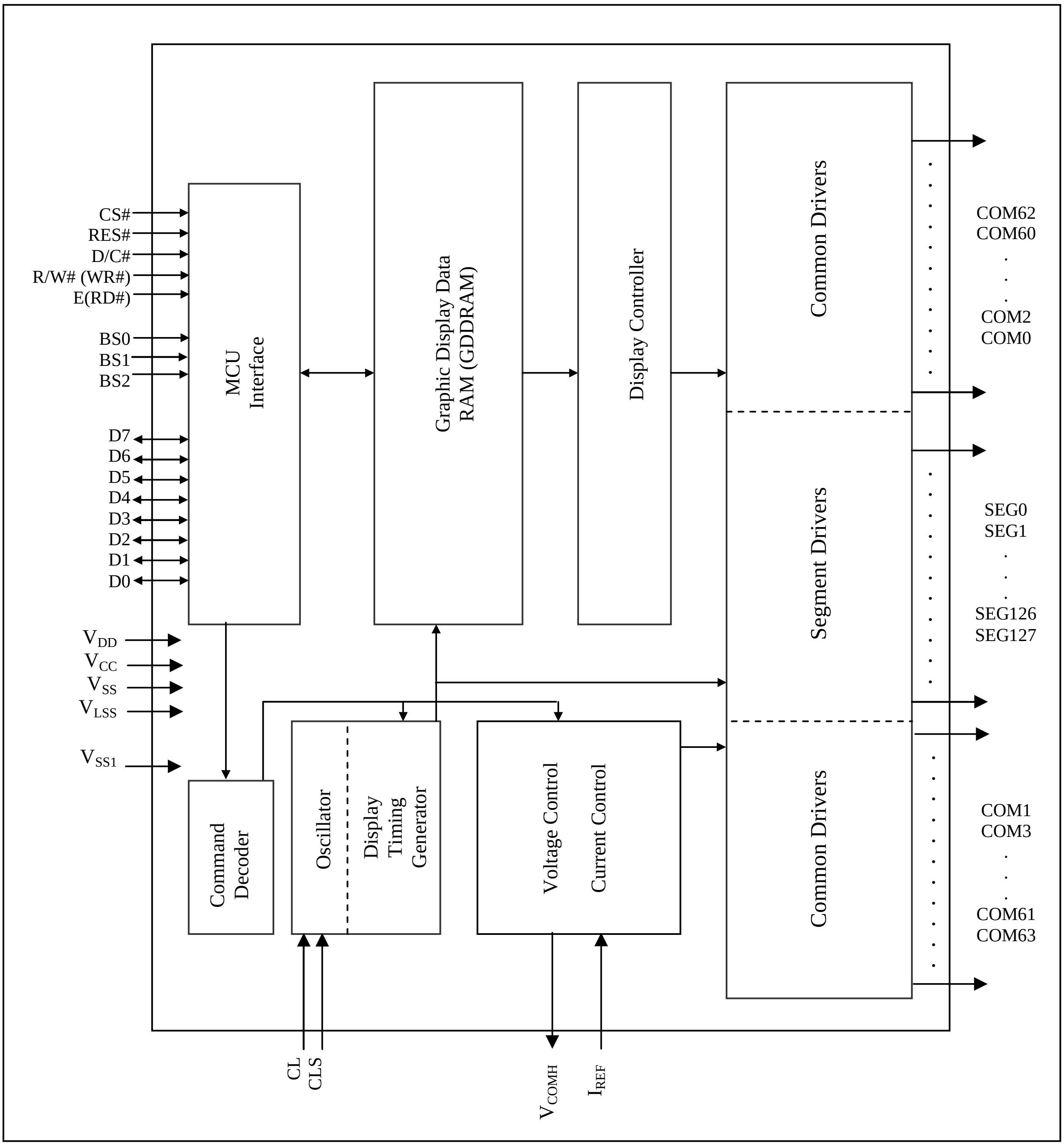
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1309Z	128	64	COG	Page 9	o Min SEG pad pitch : 37.5um o Min COM pad pitch : 27um o Min I/O pad pitch : 60 um o Die thickness : 300 +/- 15 um
SSD1309UR1	128	64	COF	Page 11,61	o 35mm film, 4 sprocket hole o Hot bar type COF o 8-bit 80 / 8-bit 68 / SPI / I2C interface o SEG lead pitch 0.120mm x 0.998 =0.11976mm o COM lead pitch 0.120mm x 0.998 =0.11976mm

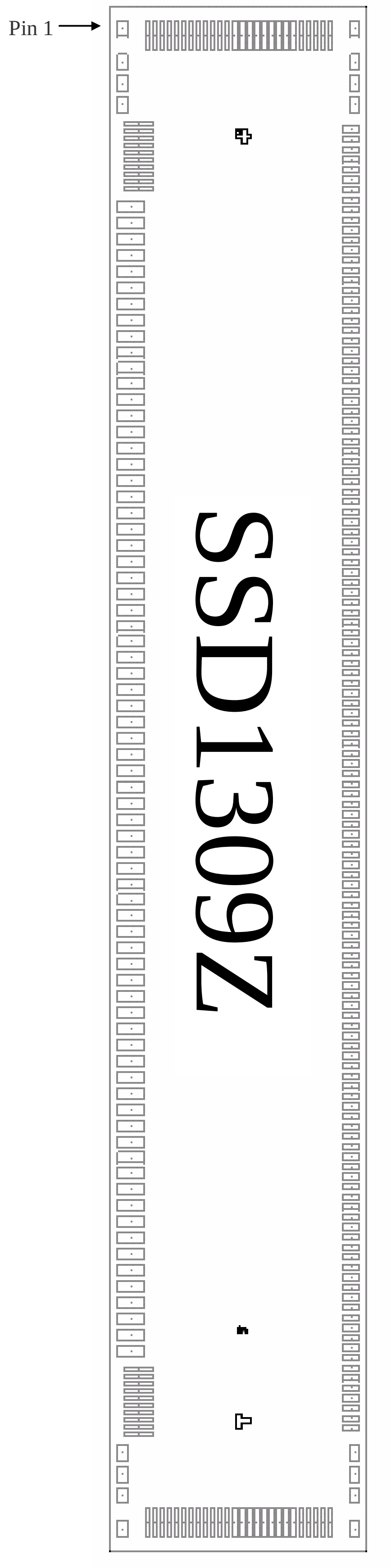
4 BLOCK DIAGRAM

Figure 4-1 : SSD1309 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1: SSD1309Z Die Drawing

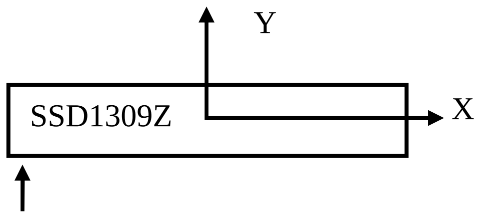


Die size (after sawing)	5.8 ± 0.05mm x 1.0 ± 0.05mm
Die thickness	300 +/- 15um
Min I/O pad pitch	60um
Min SEG pad pitch	37.5um
Min COM pad pitch	27um
Bump height	Nominal 12um

Bump size		
Pad#	X[um]	Y[um]
1~4, 97~100, 127~130, 261~264	59	35
5~14, 87~96	15	108
101~126, 265~290	108	15
15~86	40	100
131~260	22	64

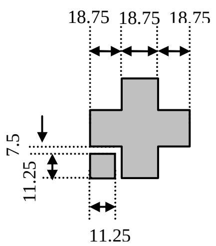
Alignment mark	Position	Size
+ shape	(-2392.2, 18.8)	56.25um x 56.25um
T shape	(2392.2, 18.8)	56.25um x 56.25um
SSL Logo	(2055, 20)	-

(For details dimension please see Figure 5-2)

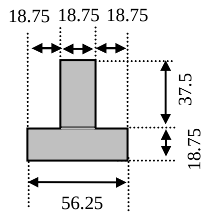


Pad 1,2,3,…->290
Gold Bumps face up

Figure 5-2: SSD1309Z alignment mark dimension



Center: (-2392.2, 18.8)
Size: 56.25 x 56.25 μm^2



Center: (2392.2, 18.8)
Size: 56.25 x 56.25 μm^2

Table 5-1: SSD1309Z Bump Die Pad Coordinates

Pin number	Pin name	X	Y
1	VCOMH	-2794.52	-431.5
2	VCOMH	-2668.32	-431.5
3	VCOMH	-2589.32	-431.5
4	VCOMH	-2510.32	-431.5
5	VLSS	-2439.76	-371.02
6	COM56	-2412.76	-371.02
7	COM57	-2385.76	-371.02
8	COM58	-2358.76	-371.02
9	COM59	-2331.76	-371.02
10	COM60	-2304.76	-371.02
11	COM61	-2277.76	-371.02
12	COM62	-2250.76	-371.02
13	COM63	-2223.76	-371.02
14	VCOMH	-2196.76	-371.02
15	NC	-2130	-399
16	VLSS	-2070	-399
17	VLSS	-2010	-399
18	VLSS	-1950	-399
19	NC	-1890	-399
20	VCC	-1830	-399
21	VCC	-1770	-399
22	VCC	-1710	-399
23	VCC	-1650	-399
24	VCOMH	-1590	-399
25	VCOMH	-1530	-399
26	VCOMH	-1470	-399
27	VCOMH	-1410	-399
28	NC	-1350	-399
29	VSS	-1290	-399
30	VSS	-1230	-399
31	VSS	-1170	-399
32	VDD	-1110	-399
33	VDD	-1050	-399
34	VDD	-990	-399
35	BS0	-930	-399
36	VSS	-870	-399
37	BS1	-810	-399
38	VDD	-750	-399
39	BS2	-690	-399
40	VSS	-630	-399
41	TR7	-570	-399
42	VSS1	-510	-399
43	CL	-450	-399
44	VSS	-390	-399
45	CS#	-330	-399
46	RES#	-270	-399
47	D/C#	-210	-399
48	VSS	-150	-399
49	R/W#(WR#)	-90	-399
50	E(RD#)	-30	-399
51	D0	30	-399
52	D1	90	-399
53	D2	150	-399
54	D3	210	-399
55	VSS	270	-399
56	D4	330	-399
57	D5	390	-399
58	D6	450	-399
59	D7	510	-399
60	IREF	570	-399
61	VSS	630	-399
62	CLS	690	-399
63	VDD	750	-399
64	VDD	810	-399
65	VCOMH	870	-399
66	VCOMH	930	-399
67	VCOMH	990	-399
68	VCOMH	1050	-399
69	VCC	1110	-399
70	VCC	1170	-399
71	VCC	1230	-399
72	VCC	1290	-399
73	VCC	1350	-399
74	NC	1410	-399
75	VLSS	1470	-399
76	VLSS	1530	-399
77	VLSS	1590	-399
78	TR6	1650	-399
79	TR5	1710	-399
80	TR4	1770	-399
81	VSS	1830	-399
82	TR3	1890	-399
83	TR2	1950	-399
84	TR1	2010	-399
85	TR0	2070	-399
86	VCC	2130	-399
87	VCOMH	2196.76	-371.02
88	COM31	2223.76	-371.02
89	COM30	2250.76	-371.02
90	COM29	2277.76	-371.02
91	COM28	2304.76	-371.02
92	COM27	2331.76	-371.02
93	COM26	2358.76	-371.02
94	COM25	2385.76	-371.02
95	COM24	2412.76	-371.02
96	VLSS	2439.76	-371.02
97	VCOMH	2510.32	-431.5
98	VCOMH	2589.32	-431.5
99	VCOMH	2668.32	-431.5
100	VCOMH	2794.52	-431.5
101	VCOMH	2770.02	-337.5
102	COM23	2770.02	-310.5
103	COM22	2770.02	-283.5
104	COM21	2770.02	-256.5
105	COM20	2770.02	-229.5
106	COM19	2770.02	-202.5
107	COM18	2770.02	-175.5
108	COM17	2770.02	-148.5
109	COM16	2770.02	-121.5
110	COM15	2770.02	-94.5
111	COM14	2770.02	-67.5
112	COM13	2770.02	-40.5
113	COM12	2770.02	-13.5
114	COM11	2770.02	13.5
115	COM10	2770.02	40.5
116	COM9	2770.02	67.5
117	COM8	2770.02	94.5
118	COM7	2770.02	121.5
119	COM6	2770.02	148.5
120	COM5	2770.02	175.5
121	COM4	2770.02	202.5
122	COM3	2770.02	229.5
123	COM2	2770.02	256.5
124	COM1	2770.02	283.5
125	COM0	2770.02	310.5
126	VSS	2770.02	337.5
127	VCOMH	2794.52	431.5
128	VCC	2668.32	431.5
129	VCC	2589.32	431.5
130	VCC	2510.32	431.5
131	VCC	2418.75	417
132	SEG0	2381.25	417
133	SEG1	2343.75	417
134	SEG2	2306.25	417
135	SEG3	2268.75	417
136	SEG4	2231.25	417
137	SEG5	2193.75	417
138	SEG6	2156.25	417
139	SEG7	2118.75	417
140	SEG8	2081.25	417
141	SEG9	2043.75	417
142	SEG10	2006.25	417
143	SEG11	1968.75	417
144	SEG12	1931.25	417
145	SEG13	1893.75	417
146	SEG14	1856.25	417
147	SEG15	1818.75	417
148	SEG16	1781.25	417
149	SEG17	1743.75	417
150	SEG18	1706.25	417
151	SEG19	1668.75	417
152	SEG20	1631.25	417
153	SEG21	1593.75	417
154	SEG22	1556.25	417
155	SEG23	1518.75	417
156	SEG24	1481.25	417
157	SEG25	1443.75	417
158	SEG26	1406.25	417
159	SEG27	1368.75	417
160	SEG28	1331.25	417
161	SEG29	1293.75	417
162	SEG30	1256.25	417
163	SEG31	1218.75	417
164	SEG32	1181.25	417
165	SEG33	1143.75	417
166	SEG34	1106.25	417
167	SEG35	1068.75	417
168	SEG36	1031.25	417
169	SEG37	993.75	417
170	SEG38	956.25	417
171	SEG39	918.75	417
172	SEG40	881.25	417
173	SEG41	843.75	417
174	SEG42	806.25	417
175	SEG43	768.75	417
176	SEG44	731.25	417
177	SEG45	693.75	417
178	SEG46	656.25	417
179	SEG47	618.75	417
180	SEG48	581.25	417
181	SEG49	543.75	417
182	SEG50	506.25	417
183	SEG51	468.75	417
184	SEG52	431.25	417
185	SEG53	393.75	417
186	SEG54	356.25	417
187	SEG55	318.75	417
188	SEG56	281.25	417
189	SEG57	243.75	417
190	SEG58	206.25	417
191	SEG59	168.75	417
192	SEG60	131.25	417
193	SEG61	93.75	417
194	SEG62	56.25	417
195	SEG63	18.75	417
196	SEG64	-18.75	417
197	SEG65	-56.25	417
198	SEG66	-93.75	417
199	SEG67	-131.25	417
200	SEG68	-168.75	417
201	SEG69	-206.25	417
202	SEG70	-243.75	417
203	SEG71	-281.25	417
204	SEG72	-318.75	417
205	SEG73	-356.25	417
206	SEG74	-393.75	417
207	SEG75	-431.25	417
208	SEG76	-468.75	417
209	SEG77	-506.25	417
210	SEG78	-543.75	417
211	SEG79	-581.25	417
212	SEG80	-618.75	417
213	SEG81	-656.25	417
214	SEG82	-693.75	417
215	SEG83	-731.25	417
216	SEG84	-768.75	417
217	SEG85	-806.25	417
218	SEG86	-843.75	417
219	SEG87	-881.25	417
220	SEG88	-918.75	417
221	SEG89	-956.25	417
222	SEG90	-993.75	417
223	SEG91	-1031.25	417
224	SEG92	-1068.75	417
225	SEG93	-1106.25	417
226	SEG94	-1143.75	417
227	SEG95	-1181.25	417
228	SEG96	-1218.75	417
229	SEG97	-1256.25	417
230	SEG98	-1293.75	417
231	SEG99	-1331.25	417
232	SEG100	-1368.75	417
233	SEG101	-1406.25	417
234	SEG102	-1443.75	417
235	SEG103	-1481.25	417
236	SEG104	-1518.75	417
237	SEG105	-1556.25	417
238	SEG106	-1593.75	417
239	SEG107	-1631.25	417
240	SEG108	-1668.75	417
241	SEG109	-1706.25	417
242	SEG110	-1743.75	417
243	SEG111	-1781.25	417
244	SEG112	-1818.75	417
245	SEG113	-1856.25	417
246	SEG114	-1893.75	417
247	SEG115	-1931.25	417
248	SEG116	-1968.75	417
249	SEG117	-2006.25	417
250	SEG118	-2043.75	417
251	SEG119	-2081.25	417
252	SEG120	-2118.75	417
253	SEG121	-2156.25	417
254	SEG122	-2193.75	417
255	SEG123	-2231.25	417
256	SEG124	-2268.75	417
257	SEG125	-2306.25	417
258	SEG126	-2343.75	417
259	SEG127	-2381.25	417
260	VCC	-2418.75	417
261	VCC	-2510.32	431.5
262	VCC	-2589.32	431.5
263	VCC	-2668.32	431.5
264	VCOMH	-2794.52	431.5
265	VSS	-2770.02	337.5
266	COM32	-2770.02	310.5
267	COM33	-2770.02	283.5
268	COM34	-2770.02	256.5
269	COM35	-2770.02	229.5
270	COM36	-2770.02	202.5
271	COM37	-2770.02	175.5
272	COM38	-2770.02	148.5
273	COM39	-2770.02	121.5
274	COM40	-2770.02	94.5
275	COM41	-2770.02	67.5
276	COM42	-2770.02	40.5
277	COM43	-2770.02	13.5
278	COM44	-2770.02	-13.5
279	COM45	-2770.02	-40.5
280	COM46	-2770.02	-67.5
281	COM47	-2770.02	-94.5
282	COM48	-2770.02	-121.5
283	COM49	-2770.02	-148.5
284	COM50	-2770.02	-175.5
285	COM51	-2770.02	-202.5
286	COM52	-2770.02	-229.5
287	COM53	-2770.02	-256.5
288	COM54	-2770.02	-283.5
289	COM55	-2770.02	-310.5
290	VCOMH	-2770.02	-337.5

6 PIN ARRANGEMENT

6.1 SSD1309UR1 pin assignment

Figure 6-1 : SSD1309UR1 Pin Assignment

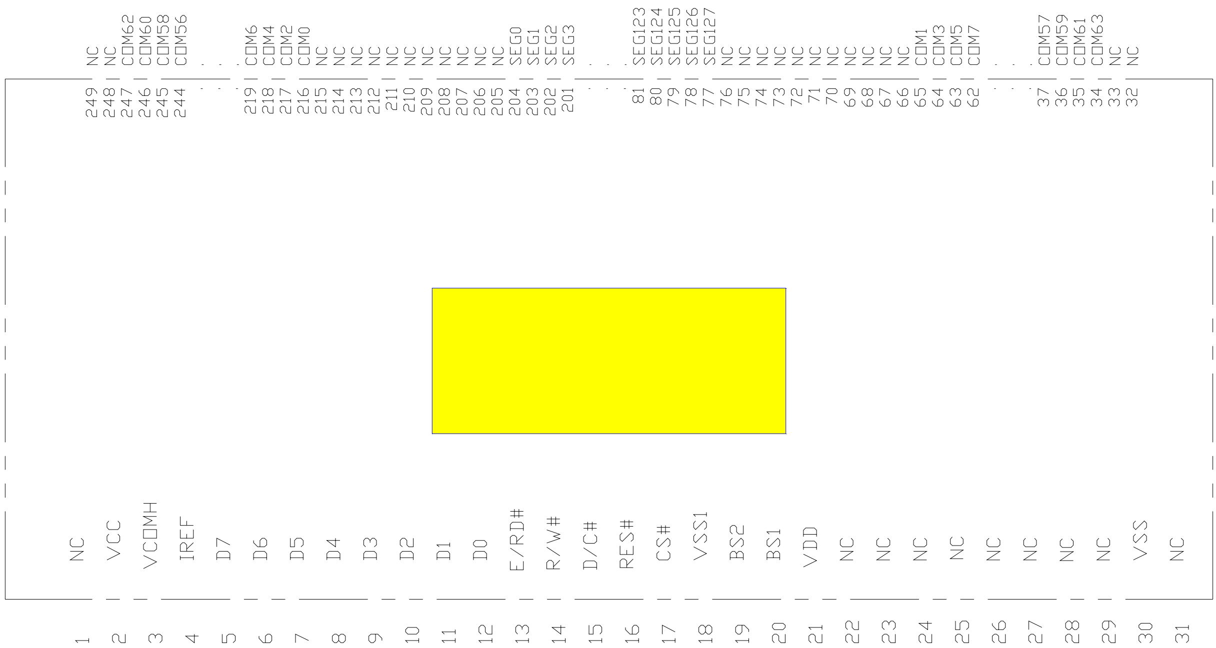


Table 6-1 : SSD1309UR1 Pin Assignment Table

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	NC	81	SEG123	161	SEG43	241	COM50
2	VCC	82	SEG122	162	SEG42	242	COM52
3	VCOMH	83	SEG121	163	SEG41	243	COM54
4	IREF	84	SEG120	164	SEG40	244	COM56
5	D7	85	SEG119	165	SEG39	245	COM58
6	D6	86	SEG118	166	SEG38	246	COM60
7	D5	87	SEG117	167	SEG37	247	COM62
8	D4	88	SEG116	168	SEG36	248	NC
9	D3	89	SEG115	169	SEG35	249	NC
10	D2	90	SEG114	170	SEG34		
11	D1	91	SEG113	171	SEG33		
12	D0	92	SEG112	172	SEG32		
13	E(RD#)	93	SEG111	173	SEG31		
14	R/W#	94	SEG110	174	SEG30		
15	D/C#	95	SEG109	175	SEG29		
16	RES#	96	SEG108	176	SEG28		
17	CS#	97	SEG107	177	SEG27		
18	VSS1	98	SEG106	178	SEG26		
19	BS2	99	SEG105	179	SEG25		
20	BS1	100	SEG104	180	SEG24		
21	VDD	101	SEG103	181	SEG23		
22	NC	102	SEG102	182	SEG22		
23	NC	103	SEG101	183	SEG21		
24	NC	104	SEG100	184	SEG20		
25	NC	105	SEG99	185	SEG19		
26	NC	106	SEG98	186	SEG18		
27	NC	107	SEG97	187	SEG17		
28	NC	108	SEG96	188	SEG16		
29	NC	109	SEG95	189	SEG15		
30	VSS	110	SEG94	190	SEG14		
31	NC	111	SEG93	191	SEG13		
32	NC	112	SEG92	192	SEG12		
33	NC	113	SEG91	193	SEG11		
34	COM63	114	SEG90	194	SEG10		
35	COM61	115	SEG89	195	SEG9		
36	COM59	116	SEG88	196	SEG8		
37	COM57	117	SEG87	197	SEG7		
38	COM55	118	SEG86	198	SEG6		
39	COM53	119	SEG85	199	SEG5		
40	COM51	120	SEG84	200	SEG4		
41	COM49	121	SEG83	201	SEG3		
42	COM47	122	SEG82	202	SEG2		
43	COM45	123	SEG81	203	SEG1		
44	COM43	124	SEG80	204	SEG0		
45	COM41	125	SEG79	205	NC		
46	COM39	126	SEG78	206	NC		
47	COM37	127	SEG77	207	NC		
48	COM35	128	SEG76	208	NC		
49	COM33	129	SEG75	209	NC		
50	COM31	130	SEG74	210	NC		
51	COM29	131	SEG73	211	NC		
52	COM27	132	SEG72	212	NC		
53	COM25	133	SEG71	213	NC		
54	COM23	134	SEG70	214	NC		
55	COM21	135	SEG69	215	NC		
56	COM19	136	SEG68	216	COM0		
57	COM17	137	SEG67	217	COM2		
58	COM15	138	SEG66	218	COM4		
59	COM13	139	SEG65	219	COM6		
60	COM11	140	SEG64	220	COM8		
61	COM9	141	SEG63	221	COM10		
62	COM7	142	SEG62	222	COM12		
63	COM5	143	SEG61	223	COM14		
64	COM3	144	SEG60	224	COM16		
65	COM1	145	SEG59	225	COM18		
66	NC	146	SEG58	226	COM20		
67	NC	147	SEG57	227	COM22		
68	NC	148	SEG56	228	COM24		
69	NC	149	SEG55	229	COM26		
70	NC	150	SEG54	230	COM28		
71	NC	151	SEG53	231	COM30		
72	NC	152	SEG52	232	COM32		
73	NC	153	SEG51	233	COM34		
74	NC	154	SEG50	234	COM36		
75	NC	155	SEG49	235	COM38		
76	NC	156	SEG48	236	COM40		
77	SEG127	157	SEG47	237	COM42		
78	SEG126	158	SEG46	238	COM44		
79	SEG125	159	SEG45	239	COM46		
80	SEG124	160	SEG44	240	COM48		

7 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DD}
P = Power pin	

Table 7-1 : SSD1309 Pin Description

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>V_{DD}</td><td>P</td><td>Power supply pin for core logic operation.</td></tr>
<tr><td>V_{CC}</td><td>P</td><td>Power supply for panel driving voltage. This is also the most positive power voltage supply pin.</td></tr>
<tr><td>V_{SS}</td><td>P</td><td>Ground pin. It must be connected to external ground.</td></tr>
<tr><td>V_{LSS}</td><td>P</td><td>Analog system ground pin. It must be connected to external ground.</td></tr>
<tr><td>V_{SS1}</td><td>-</td><td>Reserved Pin. It must be connected to external ground.</td></tr>
<tr><td>V_{COMH}</td><td>P</td><td>COM signal deselected voltage level.
A capacitor should be connected between this pin and V_{SS}.</td></tr>
<tr><td>BS[2:0]</td><td>I</td><td>MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select.

Table 7-2 : Bus Interface selection
<table>
<tr><td>BS[2:0]</td><td>Interface</td></tr>
<tr><td>000</td><td>4 line SPI</td></tr>
<tr><td>001</td><td>3 line SPI</td></tr>
<tr><td>010</td><td>I^2C</td></tr>
<tr><td>110</td><td>8-bit 8080 parallel</td></tr>
<tr><td>100</td><td>8-bit 6800 parallel</td></tr>
</table>
Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DD}</td></tr>
<tr><td>I_{REF}</td><td>I</td><td>This pin is the segment output current reference pin.

I_{REF} is supplied externally.
A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA. Please refer to Figure 8-15 for the details of resistor value</td></tr>
<tr><td>CL</td><td>I</td><td>This is external clock input pin.

When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.</td></tr>
<tr><td>CLS</td><td>I</td><td>This is internal clock enable pin.

When it is pulled HIGH (i.e. connect to V_{DD}), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.</td></tr>
</table>

Pin Name	Pin Type	Description
CS#	I	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I^2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V_{SS}. For detail relationship to MCU interface signals, refer to Timing Characteristics Diagrams Figure 13-1 to Figure 13-5
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
D[7:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
SEG0 ~ SEG127	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF.
COM0 ~ COM63	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.
TR[7:0]	-	Reserved pin and is recommended to keep it float.
NC	-	This is dummy pin. Do not group or short NC pins together.

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface selection

SSD1309 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 7-2 for BS[2:0] setting).

Table 8-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

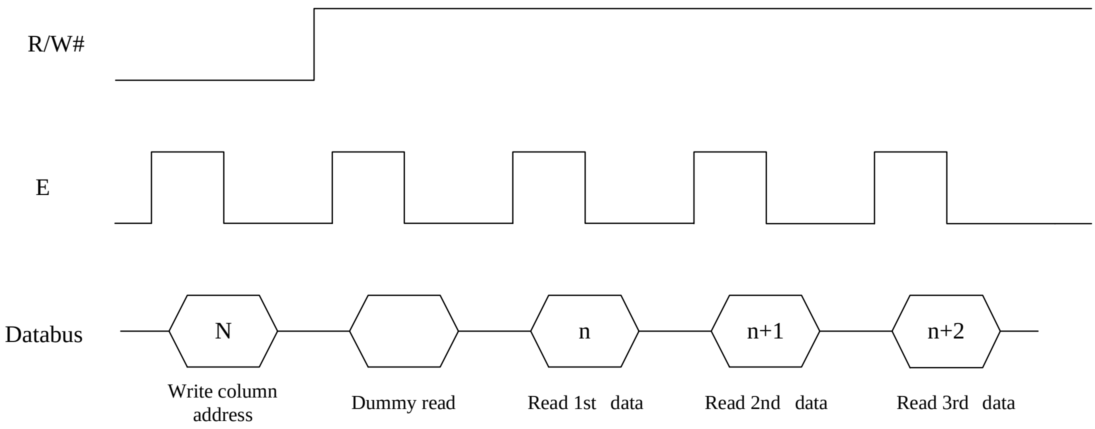
Table 8-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

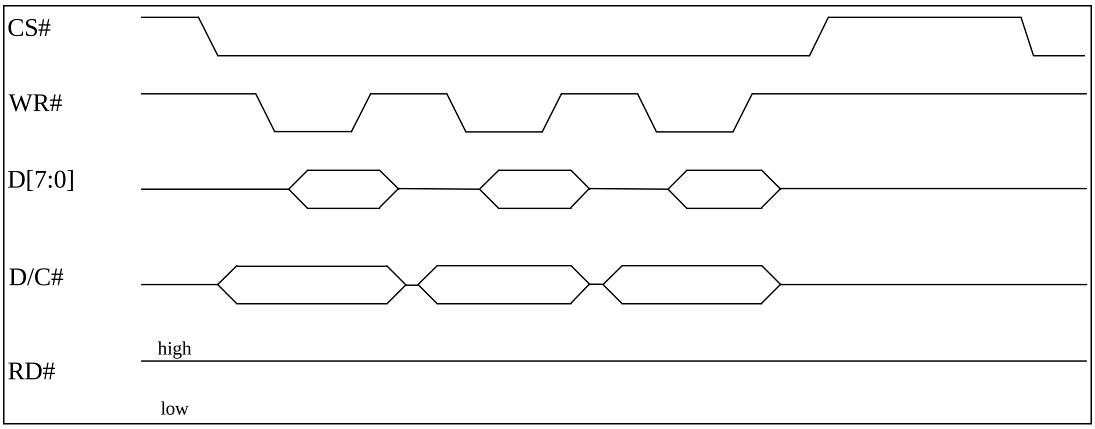


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

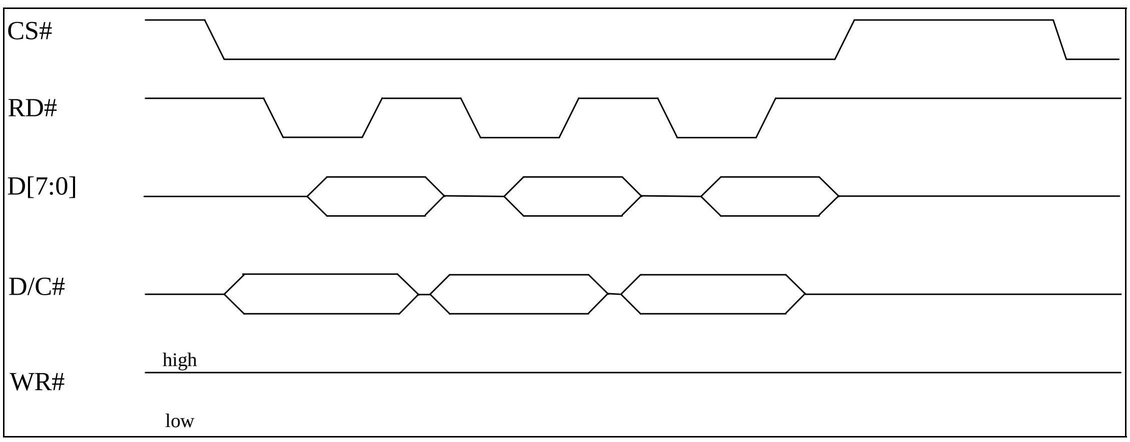


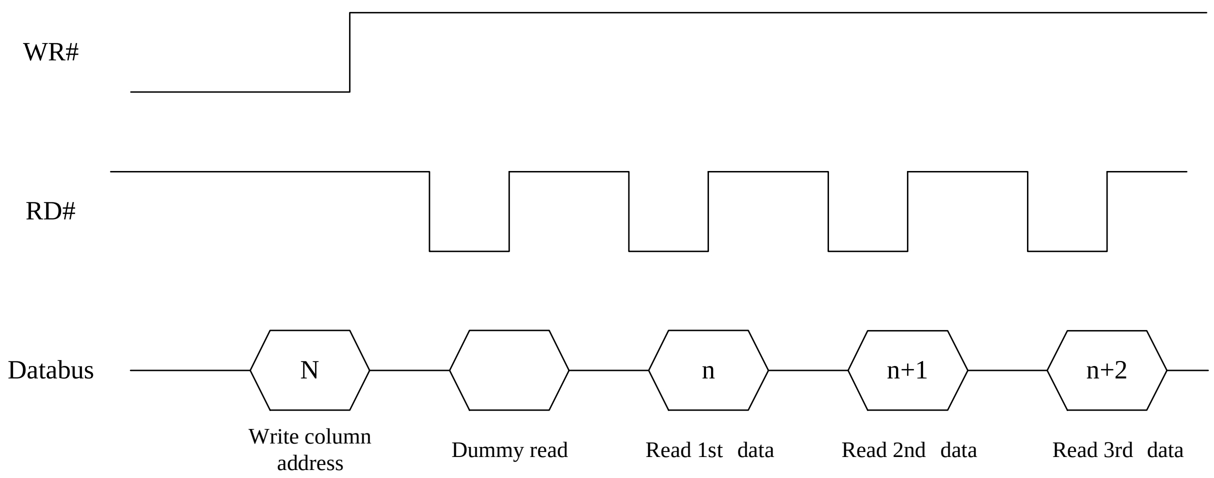
Table 8-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# (WR#)# can be connected to an external ground.

Table 8-4 : Control pins of 4-wire Serial interface

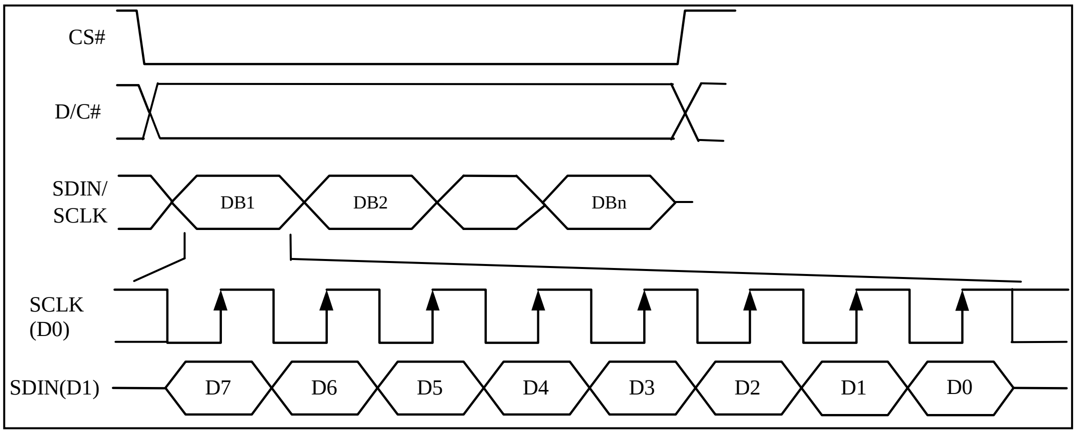
Function	E	R/W#	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal
(3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in 4-wire Serial interface mode



8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#)#, E and D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

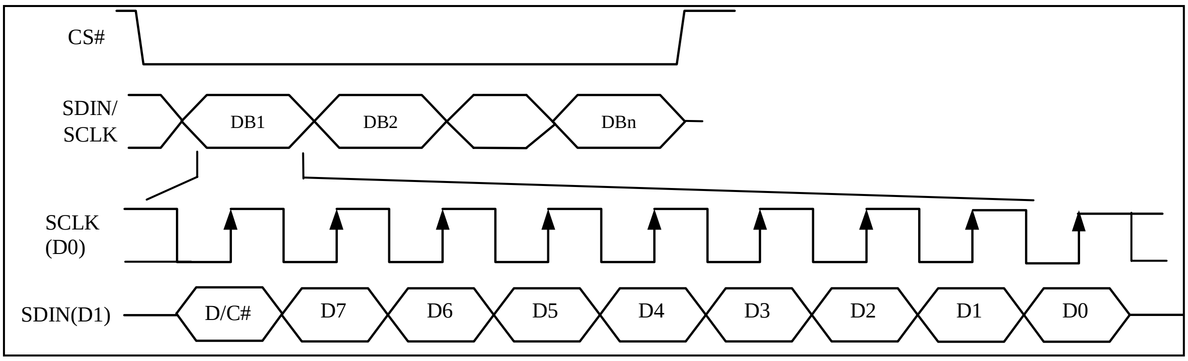
Under serial mode, only write operations are allowed.

Table 8-5 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal
(2) ↑ stands for rising edge of signal

Figure 8-6 : Write procedure in 3-wire Serial interface mode



8.1.5 MCU I^2C Interface

The I^2C communication interface consists of slave address bit SA0, I^2C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I^2C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
   SSD1309 has to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

   b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
   0 1 1 1 1 0 SA0 R/W#

   "SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1309. D/C# pin acts as SA0 for slave address selection.
   "R/W#" bit is used to determine the operation mode of the I^2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I^2C-bus data signal (SDA)
   SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

   It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

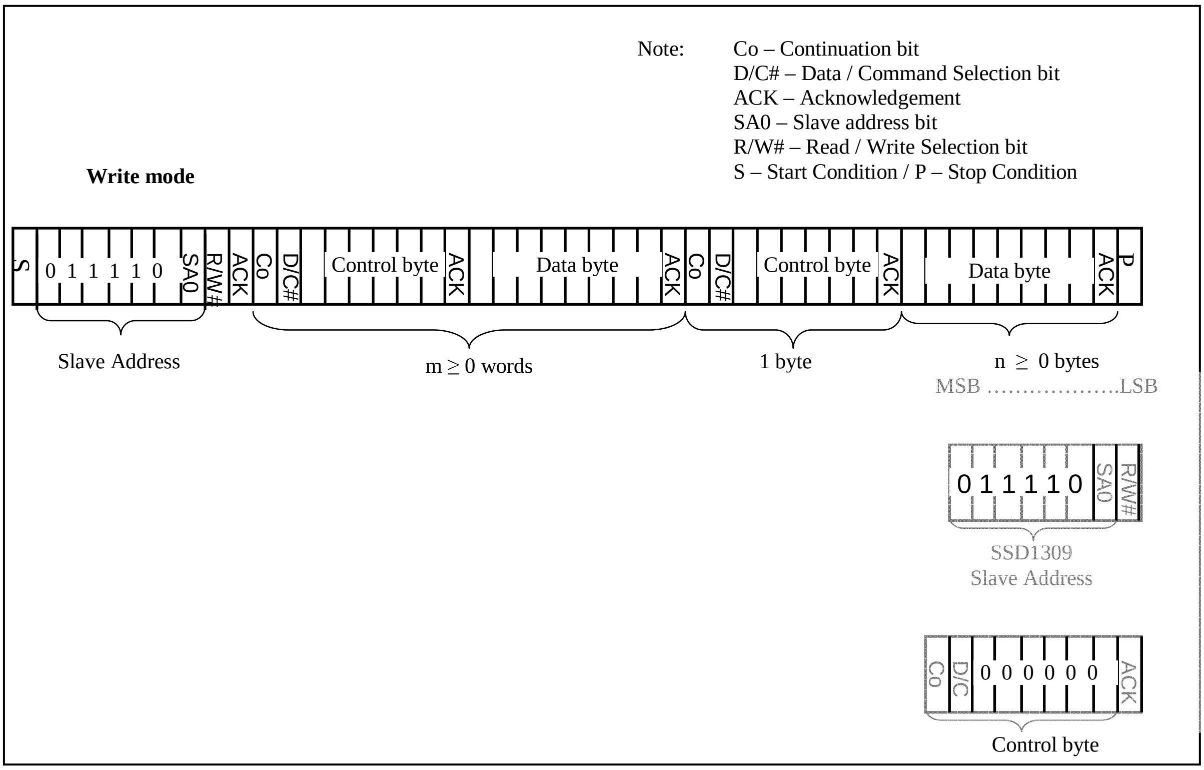
   "SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I^2C-bus.

c) I^2C-bus clock signal (SCL)
   The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

8.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 8-7 for the write mode of I²C-bus in chronological order.

Figure 8-7 : I²C-bus data format



8.1.5.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 8-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1309, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic “0”.
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 8-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
    a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 8-8. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure 8-8 : Definition of the Start and Stop Condition

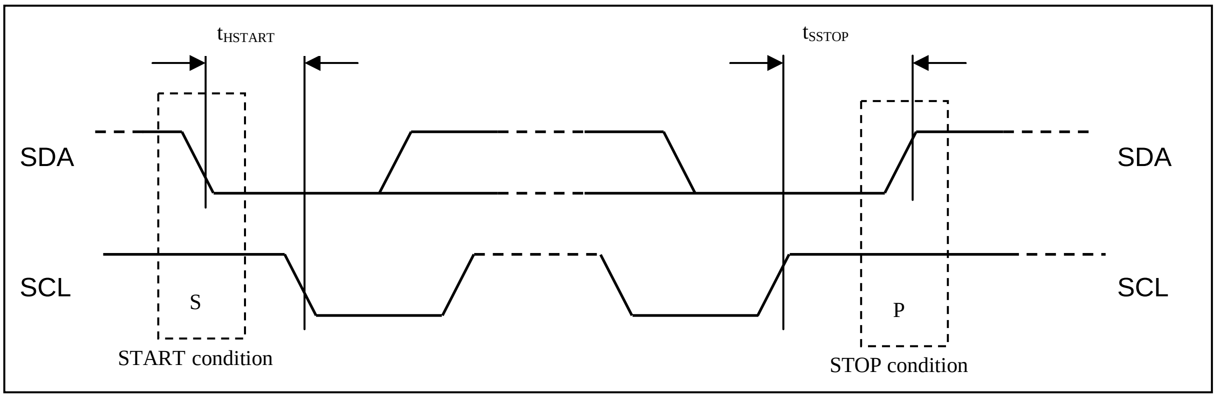
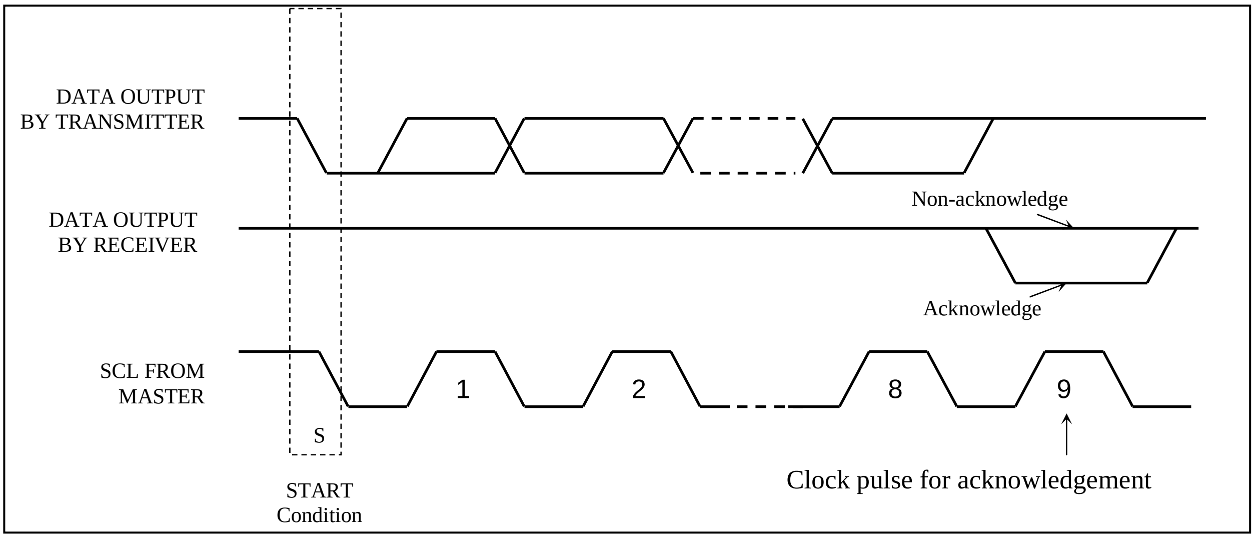


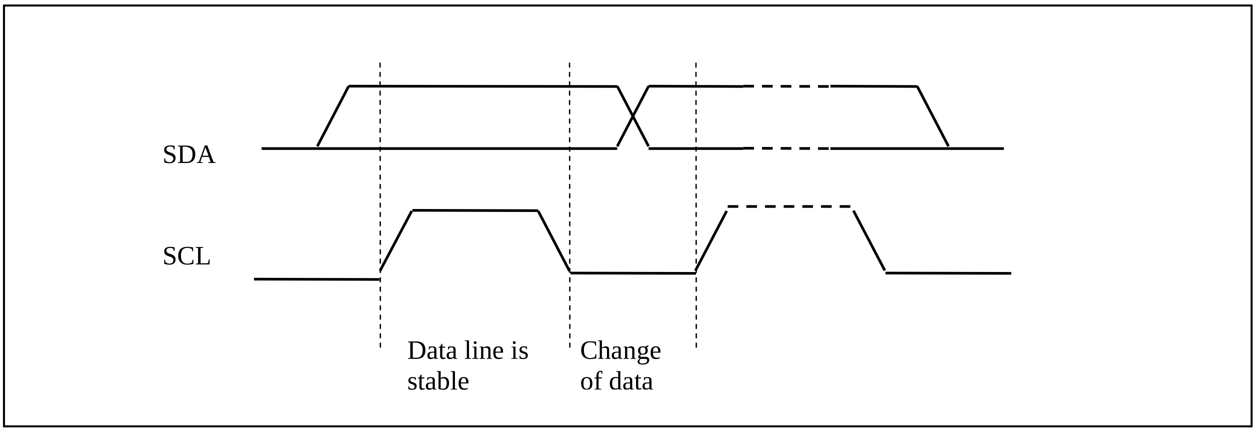
Figure 8-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 8-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 8-10 : Definition of the data transfer condition



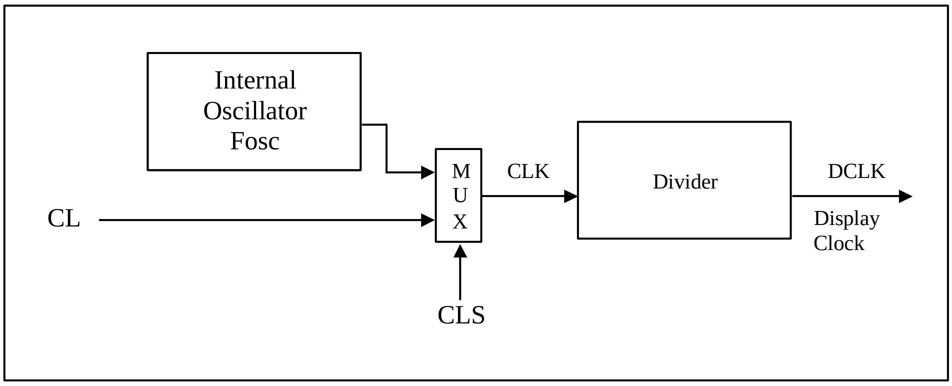
8.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

8.3 Oscillator Circuit and Display Time Generator

Figure 8-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + K_o
  = 2 + 2 + 65 = 69 at power on reset (that is K_o is a constant that equals to 65)
  (Please refer to Section 8.5 "Segment Drivers / Common Drivers" for the details of the "Phase")
- Number of multiplex ratio is set by command A8h. The power on reset value is 63 (i.e. 64MUX).
- F_{OSC} is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

8.4 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 64 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

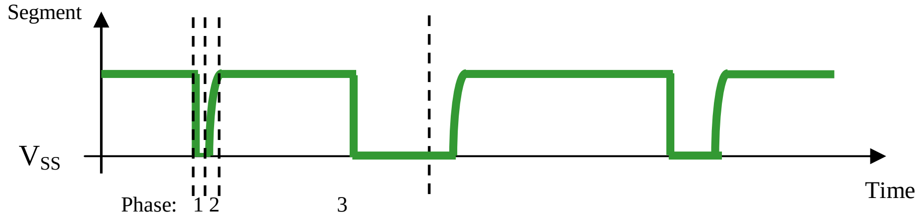
8.5 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted from 0 to 320uA with 256 steps. Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS}. The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 8-12 : Segment Output Waveform in three phases



After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 65, after finishing 65 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

8.6 Graphic Display Data RAM (GDDRAM)

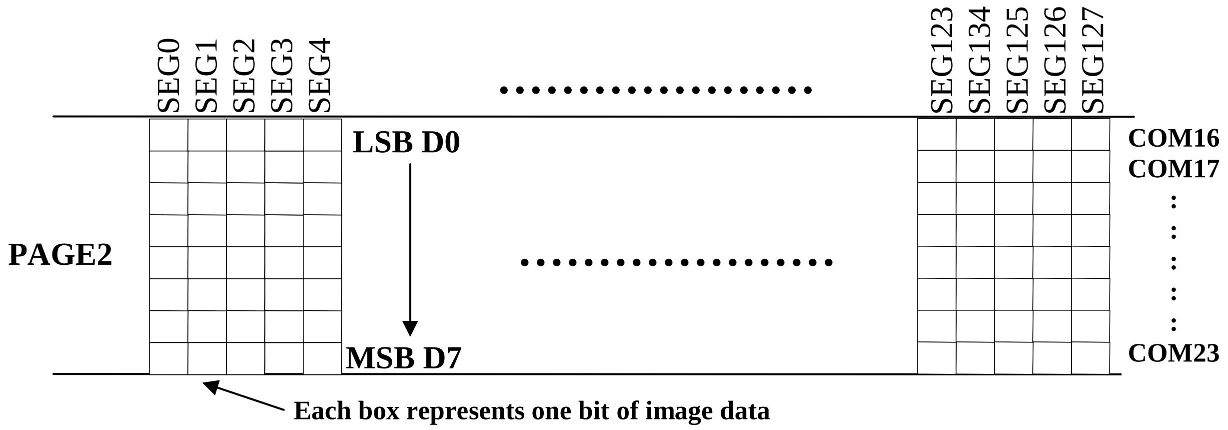
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in Figure 8-13.

Figure 8-13 : GDDRAM pages structure of SSD1309

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM 63-COM56)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM 55-COM48)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM47-COM40)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM39-COM32)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM31-COM24)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM23-COM16)
PAGE6 (COM48–COM55)	Page 6	PAGE6 (COM15-COM8)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM 7-COM0)
	SEG0 --SEG127	
Column re-mapping	SEG127 --SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 8-14.

Figure 8-14 : Enlargement of GDDRAM (No row re-mapping and column-remapping)



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 8-13.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

8.7 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

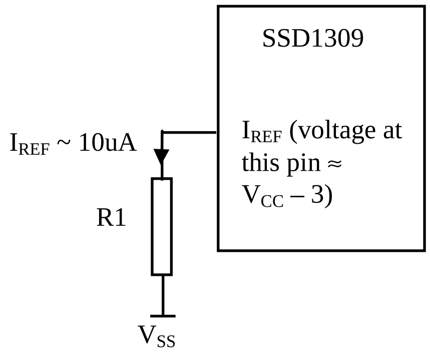
- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

  I_{SEG} = (Contrast+1) /8 x I_{REF}

  in which the contrast (0~255) is set by Set Contrast command 81h

The magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 8-15. It is recommended to set I_{REF} to 10 ± 2uA so as to achieve I_{SEG} = 320uA at maximum contrast 255.

Figure 8-15 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 3V, the value of resistor R1 can be found as below:

For I_{REF} = 10uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
≈ (12 – 3) / 10uA
= 900kΩ

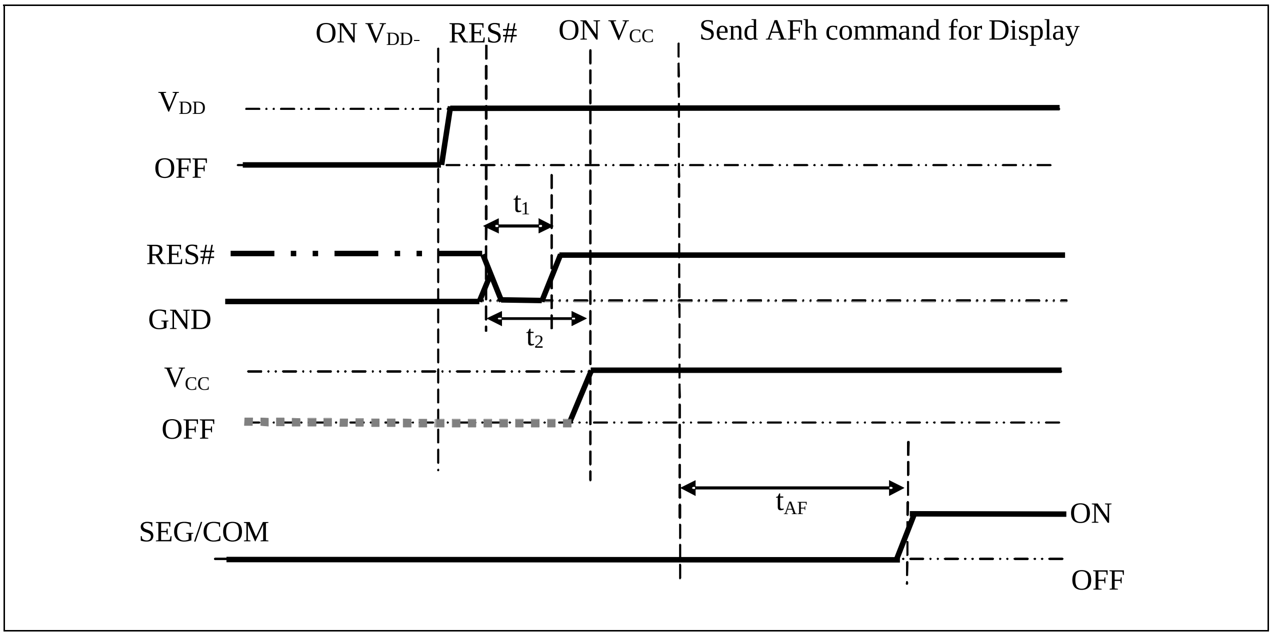
8.8 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1309

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) (3) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}. (1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

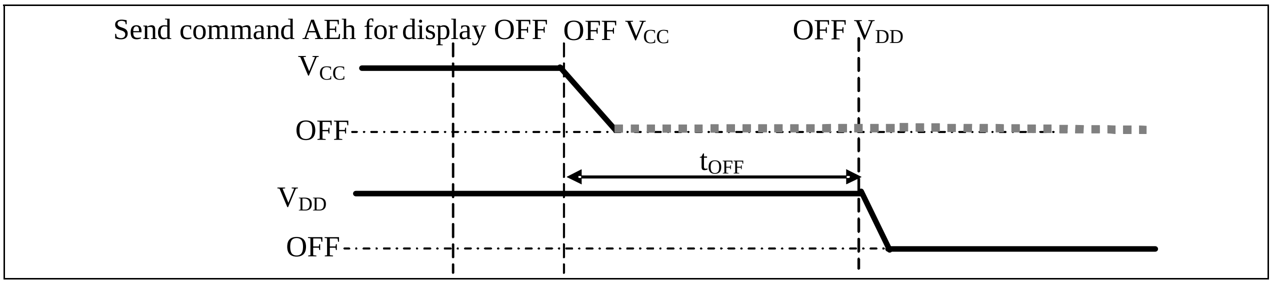
Figure 8-16 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. (1), (2)
3. Power OFF V_{DD} after t_{OFF}. (4) (where Minimum t_{OFF}=0ms, typical t_{OFF}=100ms)

Figure 8-17 : The Power OFF sequence



Note:

(1) V_{CC} should be kept float (i.e. disable) when it is OFF.

(2) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

(3) The register values are reset after t_1.

(4) V_{DD} should not be Power OFF before V_{CC} Power OFF.

9 Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

9.1 Fundamental Command Table

Table 9-1: Fundamental Command Table

1. Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE/AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation
0 0	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A_2	0 1	1 0	Set Command Lock	A[2]: MCU protection status. A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET) A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command

9.2 Scrolling Command Table

Table 9-2: Scrolling Command Table

<table>
<tr><th colspan="12">2. Scrolling Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>26/27</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>X_0</td><td rowspan="8">Continuous Horizontal Scroll Setup</td><td rowspan="8">26h, X[0]=0, Right Horizontal Scroll
27h, X[0]=1, Left Horizontal Scroll

A[7:0] : Dummy byte (Set as 00h)
Horizontal scroll by 1 column

B[2:0] : Define start page address<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>
C[2:0] : Set time interval between each scroll step in terms of frame frequency<table><tr><td>000b – 5 frames</td><td>100b – 2 frames</td></tr><tr><td>001b – 64 frames</td><td>101b – 3 frames</td></tr><tr><td>010b – 128 frames</td><td>110b – 4 frames</td></tr><tr><td>011b – 256 frames</td><td>111b – 1 frames</td></tr></table>
D[2:0] : Define end page address<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>
E[7:0] : Dummy byte (Set as 00h)

F[7:0] : Define the start column (RESET = 00h)

G[7:0] : Define the end column address (RESET = 7Fh)

Notes:
(1) The value of D[2:0] must be larger than or equal to B[2:0]
(2) The value of G[7:0] must be larger than or equal to F[7:0]</td></tr>
<tr><td>0</td><td>A[7:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>B[2:0]</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>C[2:0]</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td>0</td><td>D[2:0]</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>D_2</td><td>D_1</td><td>D_0</td></tr>
<tr><td>0</td><td>E[7:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>F[7:0]</td><td>F_7</td><td>F_6</td><td>F_5</td><td>F_4</td><td>F_3</td><td>F_2</td><td>F_1</td><td>F_0</td></tr>
<tr><td>0</td><td>G[7:0]</td><td>G_7</td><td>G_6</td><td>G_5</td><td>G_4</td><td>G_3</td><td>G_2</td><td>G_1</td><td>G_0</td></tr>
</table>

<table>
<tr><th colspan="12">2. Scrolling Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>29/2A</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>X_1</td><td>X_0</td><td rowspan="8">Continuous Vertical and Horizontal Scroll Setup</td><td rowspan="8">29h, X_1X_0=01b : Vertical and Right Horizontal Scroll
2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll

A[0] : Set number of column scroll offset
0b No horizontal scroll
1b Horizontal scroll by 1 column

B[2:0] : Define start page address
<table>
<tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr>
<tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr>
<tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr>
</table>
C[2:0] : Set time interval between each scroll step in terms of frame frequency
<table>
<tr><td>000b – 5 frames</td><td>100b – 2 frames</td></tr>
<tr><td>001b – 64 frames</td><td>101b – 3 frames</td></tr>
<tr><td>010b – 128 frames</td><td>110b – 4 frames</td></tr>
<tr><td>011b – 256 frames</td><td>111b – 1 frames</td></tr>
</table>
D[2:0] : Define end page address
<table>
<tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr>
<tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr>
<tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr>
</table>
E[5:0] : Vertical scrolling offset
e.g. E[5:0]= 01h refer to offset =1 row
E[5:0] =3Fh refer to offset =63 rows

F[7:0] : Define the start column (RESET = 00h)

G[7:0] : Define the end column address (RESET = 7Fh)

Note
(1) The value of D[2:0] must be larger than or equal to B[2:0]

(2) The value of G[7:0] must be larger than or equal to F[7:0]</td></tr>
<tr><td>0</td><td>A[0]</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>A_0</td></tr>
<tr><td>0</td><td>B[2:0]</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>C[2:0]</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td>0</td><td>D[2:0]</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>D_2</td><td>D_1</td><td>D_0</td></tr>
<tr><td>0</td><td>E[5:0]</td><td>*</td><td>*</td><td>E_5</td><td>E_4</td><td>E_3</td><td>E_2</td><td>E_1</td><td>E_0</td></tr>
<tr><td>0</td><td>F[7:0]</td><td>F_7</td><td>F_6</td><td>F_5</td><td>F_4</td><td>F_3</td><td>F_2</td><td>F_1</td><td>F_0</td></tr>
<tr><td>0</td><td>G[7:0]</td><td>G_7</td><td>G_6</td><td>G_5</td><td>G_4</td><td>G_3</td><td>G_2</td><td>G_1</td><td>G_0</td></tr>
<tr><td>0</td><td>2E</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Deactivate scroll</td><td>Stop scrolling that is configured by command 26h/27h/29h/2Ah.

Note
(1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.</td></tr>
</table>

2. Scrolling Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h; 2Fh. Valid command sequence 2: 27h; 2Fh. Valid command sequence 3: 29h; 2Fh. Valid command sequence 4: 2Ah; 2Fh. For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.
0 0 0	A3 A[5:0] B[6:0]	1 * *	0 * B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64] **Note** (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line ($X_5X_4X_3X_2X_1X_0$ of 40h~7Fh) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0]= 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls (6) When vertical scrolling is enabled by command 29h / 2Ah, the vertical scroll area is defined by this command

<table>
<tr><th colspan="12">2. Scrolling Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>2C/2D</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>X_0</td><td rowspan="8">Content Scroll Setup</td><td rowspan="8">2Ch, X[0]=0, Right Horizontal Scroll by one column

2Dh, X[0]=1, Left Horizontal Scroll by one column

A[7:0] : Dummy byte (Set as 00h)
Horizontal scroll by 1 column

B[2:0] : Define start page address<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>
C[7:0] : Dummy byte (Set as 01h)

D[2:0] : Define end page address<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>
E[7:0] : Dummy byte (Set as 00h)

F[7:0] : Define the start column (RESET = 00h)

G[7:0] : Define the end column address (RESET = 7Fh)

Note
(1) The value of D[2:0] must be larger than or equal to B[2:0]

(2) The value of G[7:0] must be larger than F[7:0]

(3) A delay time of $2/FrameFreq$ must be set if sending the command of 2Ch / 2Dh consecutively.</td></tr>
<tr><td>0</td><td>A[7:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>B[2:0]</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>C[7:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>D[2:0]</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>D_2</td><td>D_1</td><td>D_0</td></tr>
<tr><td>0</td><td>E[7:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>F[7:0]</td><td>F_7</td><td>F_6</td><td>F_5</td><td>F_4</td><td>F_3</td><td>F_2</td><td>F_1</td><td>F_0</td></tr>
<tr><td>0</td><td>G[7:0]</td><td>G_7</td><td>G_6</td><td>G_5</td><td>G_4</td><td>G_3</td><td>G_2</td><td>G_1</td><td>G_0</td></tr>
</table>

Note

(1) "*" stands for "Don't care".

9.3 Addressing Setting Command Table

Table 9-3: Addressing Setting Command Table

3. Addressing Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[7:0] : Column start address, range : 0-127d, (RESET=0d) B[7:0]: Column end address, range : 0-127d, (RESET =127d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0]. **Note** (1) This command is only for page addressing mode

9.4 Hardware Configuration (Panel resolution & layout related) Command Table

Table 9-4: Hardware Configuration (Panel resolution & layout related) Command Table

4. Hardware Configuration (Panel resolution & layout related) Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~63d The value is reset to 00h after RESET.
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b (RESET), Alternative COM pin configuration A[5]=0b (RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap
0 0	DC A[1:0]	1 0	1 0	0 0	1 0	1 0	1 0	0 A_1	0 A_0	Set GPIO	A[1:0] GPIO : 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [RESET] 11 pin output HIGH

9.5 Timing & Driving Scheme Setting Command Table

Table 9-5: Timing & Driving Scheme Setting Command Table

<table>
<tr><th colspan="12">5. Timing & Driving Scheme Setting Command Table</th></tr>
<tr><td>0
0</td><td>D5
A[7:0]</td><td>1
A_7</td><td>1
A_6</td><td>0
A_5</td><td>1
A_4</td><td>0
A_3</td><td>1
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Display Clock Divide Ratio/Oscillator Frequency</td><td>A[3:0] : Define the divide ratio (D) of the display clocks (DCLK):
Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1)

A[7:4] : Set the Oscillator Frequency, F_{OSC}.
Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b

Range:0000b~1111b
Frequency increases as setting value increases.</td></tr>
<tr><td>0
0</td><td>D9
A[7:0]</td><td>1
A_7</td><td>1
A_6</td><td>0
A_5</td><td>1
A_4</td><td>1
A_3</td><td>0
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Pre-charge Period</td><td>A[3:0] : Phase 1 period of up to 15 DCLK
Clock 0 is invalid entry
(RESET=2h)

A[7:4] : Phase 2 period of up to 15 DCLK
Clock 0 is invalid entry
(RESET=2h)</td></tr>
<tr><td>0
0</td><td>DB
A[5:2]</td><td>1
0</td><td>1
0</td><td>0
A_5</td><td>1
A_4</td><td>1
A_3</td><td>0
A_2</td><td>1
0</td><td>1
0</td><td>Set V_{COMH} Deselect Level</td><td><table><tr><th>A[5:2]</th><th>Hex code</th><th>V_{COMH} deselect level</th></tr><tr><td>0000b</td><td>00h</td><td>~ 0.64 x V_{CC}</td></tr><tr><td>1101b</td><td>34h</td><td>~ 0.78 x V_{CC} (RESET)</td></tr><tr><td>1111b</td><td>3Ch</td><td>~ 0.84 x V_{CC}</td></tr></table></td></tr>
</table>

Note

(2) "*" stands for "Don't care".

Table 9-6 : Read Command Table

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D[7] : Reserved D[6] : "1" for display OFF / "0" for display ON D[5] : Reserved D[4] : Reserved D[3] : Reserved D[2] : Reserved D[1] : Reserved D[0] : Reserved

Note

(1) Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

9.6 Data Read / Write

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.
In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.
Also, a dummy read is required before the first data read.
To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

Table 9-7 : Address increment table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

10 COMMAND DESCRIPTIONS

10.1 Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)

This command specifies the lower nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Refer to Section 9.3 and Section 10.3 for details.

10.2 Set Higher Column Start Address for Page Addressing Mode (10h~1Fh)

This command specifies the higher nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Refer to Section 9.3 and Section 10.3 for details.

10.3 Set Memory Addressing Mode (20h)

There are 3 different memory addressing mode in SSD1309: page addressing mode, horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above three modes. In there, “COL” means the graphic display data RAM column.

<u>Page addressing mode (A[1:0]=10xb)</u>

In page addressing mode, after the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. The sequence of movement of the PAGE and column address point for page addressing mode is shown in Figure 10-1.

Figure 10-1 : Address Pointer Movement of Page addressing mode

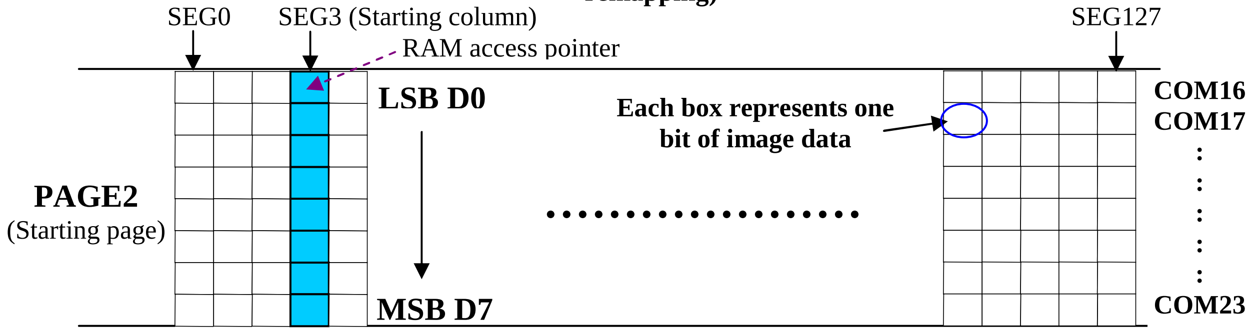
	COL0	COL 1	…..	COL 126	COL 127
PAGE0					
PAGE1					
:					
PAGE6					
PAGE7					

In normal display data RAM read or write and page addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the page start address of the target display location by command B0h to B7h.
- Set the lower start column address of pointer by command 00h~0Fh.
- Set the upper start column address of pointer by command 10h~1Fh.

For example, if the page address is set to B2h, lower column address is 03h and upper column address is 10h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 10-2. The input data byte will be written into RAM position of column 3.

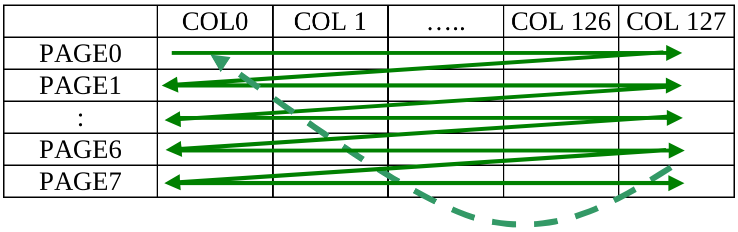
Figure 10-2 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)



Horizontal addressing mode (A[1:0]=00b)

In horizontal addressing mode, after the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is increased by 1. The sequence of movement of the page and column address point for horizontal addressing mode is shown in Figure 10-3. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-3.)

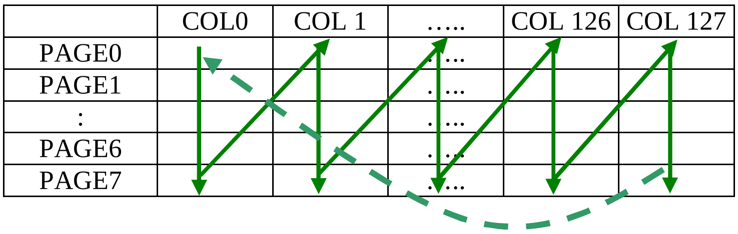
Figure 10-3 : Address Pointer Movement of Horizontal addressing mode



Vertical addressing mode: (A[1:0]=01b)

In vertical addressing mode, after the display RAM is read / written, the page address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and column address pointer is increased by 1. The sequence of movement of the page and column address point for vertical addressing mode is shown in Figure 10-4. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-4.)

Figure 10-4 : Address Pointer Movement of Vertical addressing mode



In normal display data RAM read or write and horizontal / vertical addressing mode, the following steps are required to define the RAM access pointer location:

- Set the column start and end address of the target display location by command 21h.
- Set the page start and end address of the target display location by command 22h.

Example is shown in Figure 10-5.

10.4 Set Column Address (21h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command 20h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.5 Set Page Address (22h)

This triple byte command specifies page start address and end address of the display data RAM. This command also sets the page address pointer to page start address. This pointer is used to define the current read/write page address in graphic display data RAM. If vertical address increment mode is enabled by command 20h, after finishing read/write one page data, it is incremented automatically to the next page address. Whenever the page address pointer finishes accessing the end page address, it is reset back to start page address.

The figure below shows the way of column and page address pointer movement through the example: column start address is set to 2 and column end address is set to 97, page start address is set to 1 and page end address is set to 2; Horizontal address increment mode is enabled by command 20h. In this case, the graphic display data RAM column accessible range is from column 2 to column 97 and from page 1 to page 2 only. In addition, the column address pointer is set to 2 and page address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 10-5*). Whenever the column address pointer finishes accessing the end column 97, it is reset back to column 2 and page address is automatically increased by 1 (*solid line in Figure 10-5*). While the end page 2 and end column 97 RAM location is accessed, the page address is reset back to 1 and the column address is reset back to 2 (*dotted line in Figure 10-5*). .

Figure 10-5: Example of Column and Row Address Pointer Movement (LS pin pulled LOW)

	Col 0	Col 1	Col 2	…..	…….	Col 97	Col98	……..	Col 126	Col 127
PAGE0										
PAGE1										
PAGE2										
:										
PAGE6										
PAGE7										

10.6 Set Display Start Line (40h~7Fh)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 63. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on. Refer to Table 10-1 for more illustrations.

10.7 Set Contrast Control for BANK0 (81h)

This command sets the Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current increases as the contrast step value increases.

10.8 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Refer to Section 9.4.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

10.9 Entire Display ON (A4h/A5h)

A4h command enable display outputs according to the GDDRAM contents.
If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents.
In other words, A4h command resumes the display from entire display "ON" stage.
A5h command forces the entire display to be "ON", regardless of the contents of the display data RAM.

10.10 Set Normal/Inverse Display (A6h/A7h)

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an "ON" pixel while in inverse display a RAM data of 0 indicates an "ON" pixel.

10.11 Set Multiplex Ratio (A8h)

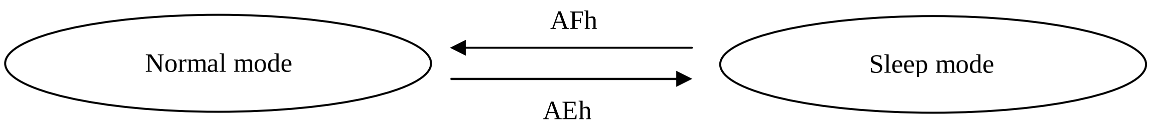
This command switches the default 64 multiplex mode to any multiplex ratio, ranging from 16 to 64. The output pads COM0~COM63 will be switched to the corresponding COM signal.

10.12 Set Display ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned OFF and the segment and common output are in V_{SS} state and high impedance state, respectively. These commands set the display to one of the two states:

- AEh : Display OFF
- AFh : Display ON

Figure 10-6 : Transition between different modes



10.13 Set Page Start Address for Page Addressing Mode (B0h~B7h)

This command positions the page start address from 0 to 7 in GDDRAM under Page Addressing Mode. Refer to Section 10.3 for details.

10.14 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped immediately. Please refer to Table 10-3 for details.

10.15 Set Display Offset (D3h)

This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM63 (assuming that COM0 is the display start line then the display start line register is equal to 0).

For example, to move the COM16 towards the COM0 direction by 16 lines the 6-bit data in the second byte should be given as 010000b. To move in the opposite direction by 16 lines the 6-bit data should be given by 64 – 16, so the second byte would be 100000b. The following two tables (Table 10-1, Table 10-2) show the examples of setting the command C0h/C8h and D3h.

Table 10-1: Example of Set Display Offset and Display Start Line without Remap

Hardware pin name	Output												
	64		64		64		56		56		56		Set MUX ration (A8h)
	Normal		Normal		Normal		Normal		Normal		Normal		COM normal / remap (C0h / C8h)
	0		8		0		0		8		0		Display offset (D3h)
	0		0		8		0		0		8		Display start line (40h - 7Fh)
COM0	ROW0	RAM0	ROW8	RAM8	ROW0	RAM8	ROW0	RAM0	ROW8	RAM8	ROW0	RAM8	
COM1	ROW1	RAM1	ROW9	RAM9	ROW1	RAM9	ROW1	RAM1	ROW9	RAM9	ROW1	RAM9	
COM2	ROW2	RAM2	ROW10	RAM10	ROW2	RAM10	ROW2	RAM2	ROW10	RAM10	ROW2	RAM10	
COM3	ROW3	RAM3	ROW11	RAM11	ROW3	RAM11	ROW3	RAM3	ROW11	RAM11	ROW3	RAM11	
COM4	ROW4	RAM4	ROW12	RAM12	ROW4	RAM12	ROW4	RAM4	ROW12	RAM12	ROW4	RAM12	
COM5	ROW5	RAM5	ROW13	RAM13	ROW5	RAM13	ROW5	RAM5	ROW13	RAM13	ROW5	RAM13	
COM6	ROW6	RAM6	ROW14	RAM14	ROW6	RAM14	ROW6	RAM6	ROW14	RAM14	ROW6	RAM14	
COM7	ROW7	RAM7	ROW15	RAM15	ROW7	RAM15	ROW7	RAM7	ROW15	RAM15	ROW7	RAM15	
COM8	ROW8	RAM8	ROW16	RAM16	ROW8	RAM16	ROW8	RAM8	ROW16	RAM16	ROW8	RAM16	
COM9	ROW9	RAM9	ROW17	RAM17	ROW9	RAM17	ROW9	RAM9	ROW17	RAM17	ROW9	RAM17	
COM10	ROW10	RAM10	ROW18	RAM18	ROW10	RAM18	ROW10	RAM10	ROW18	RAM18	ROW10	RAM18	
COM11	ROW11	RAM11	ROW19	RAM19	ROW11	RAM19	ROW11	RAM11	ROW19	RAM19	ROW11	RAM19	
COM12	ROW12	RAM12	ROW20	RAM20	ROW12	RAM20	ROW12	RAM12	ROW20	RAM20	ROW12	RAM20	
COM13	ROW13	RAM13	ROW21	RAM21	ROW13	RAM21	ROW13	RAM13	ROW21	RAM21	ROW13	RAM21	
COM14	ROW14	RAM14	ROW22	RAM22	ROW14	RAM22	ROW14	RAM14	ROW22	RAM22	ROW14	RAM22	
COM15	ROW15	RAM15	ROW23	RAM23	ROW15	RAM23	ROW15	RAM15	ROW23	RAM23	ROW15	RAM23	
COM16	ROW16	RAM16	ROW24	RAM24	ROW16	RAM24	ROW16	RAM16	ROW24	RAM24	ROW16	RAM24	
COM17	ROW17	RAM17	ROW25	RAM25	ROW17	RAM25	ROW17	RAM17	ROW25	RAM25	ROW17	RAM25	
COM18	ROW18	RAM18	ROW26	RAM26	ROW18	RAM26	ROW18	RAM18	ROW26	RAM26	ROW18	RAM26	
COM19	ROW19	RAM19	ROW27	RAM27	ROW19	RAM27	ROW19	RAM19	ROW27	RAM27	ROW19	RAM27	
COM20	ROW20	RAM20	ROW28	RAM28	ROW20	RAM28	ROW20	RAM20	ROW28	RAM28	ROW20	RAM28	
COM21	ROW21	RAM21	ROW29	RAM29	ROW21	RAM29	ROW21	RAM21	ROW29	RAM29	ROW21	RAM29	
COM22	ROW22	RAM22	ROW30	RAM30	ROW22	RAM30	ROW22	RAM22	ROW30	RAM30	ROW22	RAM30	
COM23	ROW23	RAM23	ROW31	RAM31	ROW23	RAM31	ROW23	RAM23	ROW31	RAM31	ROW23	RAM31	
COM24	ROW24	RAM24	ROW32	RAM32	ROW24	RAM32	ROW24	RAM24	ROW32	RAM32	ROW24	RAM32	
COM25	ROW25	RAM25	ROW33	RAM33	ROW25	RAM33	ROW25	RAM25	ROW33	RAM33	ROW25	RAM33	
COM26	ROW26	RAM26	ROW34	RAM34	ROW26	RAM34	ROW26	RAM26	ROW34	RAM34	ROW26	RAM34	
COM27	ROW27	RAM27	ROW35	RAM35	ROW27	RAM35	ROW27	RAM27	ROW35	RAM35	ROW27	RAM35	
COM28	ROW28	RAM28	ROW36	RAM36	ROW28	RAM36	ROW28	RAM28	ROW36	RAM36	ROW28	RAM36	
COM29	ROW29	RAM29	ROW37	RAM37	ROW29	RAM37	ROW29	RAM29	ROW37	RAM37	ROW29	RAM37	
COM30	ROW30	RAM30	ROW38	RAM38	ROW30	RAM38	ROW30	RAM30	ROW38	RAM38	ROW30	RAM38	
COM31	ROW31	RAM31	ROW39	RAM39	ROW31	RAM39	ROW31	RAM31	ROW39	RAM39	ROW31	RAM39	
COM32	ROW32	RAM32	ROW40	RAM40	ROW32	RAM40	ROW32	RAM32	ROW40	RAM40	ROW32	RAM40	
COM33	ROW33	RAM33	ROW41	RAM41	ROW33	RAM41	ROW33	RAM33	ROW41	RAM41	ROW33	RAM41	
COM34	ROW34	RAM34	ROW42	RAM42	ROW34	RAM42	ROW34	RAM34	ROW42	RAM42	ROW34	RAM42	
COM35	ROW35	RAM35	ROW43	RAM43	ROW35	RAM43	ROW35	RAM35	ROW43	RAM43	ROW35	RAM43	
COM36	ROW36	RAM36	ROW44	RAM44	ROW36	RAM44	ROW36	RAM36	ROW44	RAM44	ROW36	RAM44	
COM37	ROW37	RAM37	ROW45	RAM45	ROW37	RAM45	ROW37	RAM37	ROW45	RAM45	ROW37	RAM45	
COM38	ROW38	RAM38	ROW46	RAM46	ROW38	RAM46	ROW38	RAM38	ROW46	RAM46	ROW38	RAM46	
COM39	ROW39	RAM39	ROW47	RAM47	ROW39	RAM47	ROW39	RAM39	ROW47	RAM47	ROW39	RAM47	
COM40	ROW40	RAM40	ROW48	RAM48	ROW40	RAM48	ROW40	RAM40	ROW48	RAM48	ROW40	RAM48	
COM41	ROW41	RAM41	ROW49	RAM49	ROW41	RAM49	ROW41	RAM41	ROW49	RAM49	ROW41	RAM49	
COM42	ROW42	RAM42	ROW50	RAM50	ROW42	RAM50	ROW42	RAM42	ROW50	RAM50	ROW42	RAM50	
COM43	ROW43	RAM43	ROW51	RAM51	ROW43	RAM51	ROW43	RAM43	ROW51	RAM51	ROW43	RAM51	
COM44	ROW44	RAM44	ROW52	RAM52	ROW44	RAM52	ROW44	RAM44	ROW52	RAM52	ROW44	RAM52	
COM45	ROW45	RAM45	ROW53	RAM53	ROW45	RAM53	ROW45	RAM45	ROW53	RAM53	ROW45	RAM53	
COM46	ROW46	RAM46	ROW54	RAM54	ROW46	RAM54	ROW46	RAM46	ROW54	RAM54	ROW46	RAM54	
COM47	ROW47	RAM47	ROW55	RAM55	ROW47	RAM55	ROW47	RAM47	ROW55	RAM55	ROW47	RAM55	
COM48	ROW48	RAM48	ROW56	RAM56	ROW48	RAM56	ROW48	RAM48	-	-	ROW48	RAM56	
COM49	ROW49	RAM49	ROW57	RAM57	ROW49	RAM57	ROW49	RAM49	-	-	ROW49	RAM57	
COM50	ROW50	RAM50	ROW58	RAM58	ROW50	RAM58	ROW50	RAM50	-	-	ROW50	RAM58	
COM51	ROW51	RAM51	ROW59	RAM59	ROW51	RAM59	ROW51	RAM51	-	-	ROW51	RAM59	
COM52	ROW52	RAM52	ROW60	RAM60	ROW52	RAM60	ROW52	RAM52	-	-	ROW52	RAM60	
COM53	ROW53	RAM53	ROW61	RAM61	ROW53	RAM61	ROW53	RAM53	-	-	ROW53	RAM61	
COM54	ROW54	RAM54	ROW62	RAM62	ROW54	RAM62	ROW54	RAM54	-	-	ROW54	RAM62	
COM55	ROW55	RAM55	ROW63	RAM63	ROW55	RAM63	ROW55	RAM55	-	-	ROW55	RAM63	
COM56	ROW56	RAM56	ROW0	RAM0	ROW56	RAM0	-	-	ROW0	RAM0	-	-	
COM57	ROW57	RAM57	ROW1	RAM1	ROW57	RAM1	-	-	ROW1	RAM1	-	-	
COM58	ROW58	RAM58	ROW2	RAM2	ROW58	RAM2	-	-	ROW2	RAM2	-	-	
COM59	ROW59	RAM59	ROW3	RAM3	ROW59	RAM3	-	-	ROW3	RAM3	-	-	
COM60	ROW60	RAM60	ROW4	RAM4	ROW60	RAM4	-	-	ROW4	RAM4	-	-	
COM61	ROW61	RAM61	ROW5	RAM5	ROW61	RAM5	-	-	ROW5	RAM5	-	-	
COM62	ROW62	RAM62	ROW6	RAM6	ROW62	RAM6	-	-	ROW6	RAM6	-	-	
COM63	ROW63	RAM63	ROW7	RAM7	ROW63	RAM7	-	-	ROW7	RAM7	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		

(a)

(b)

(c)

(d)

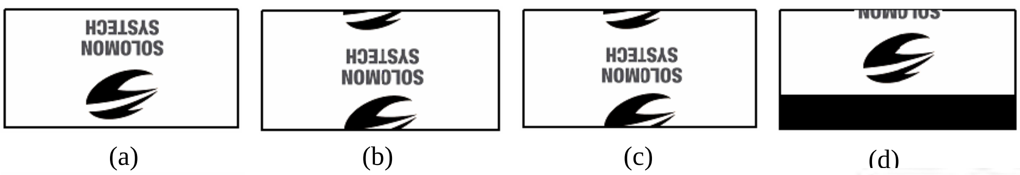
(e)

(f)

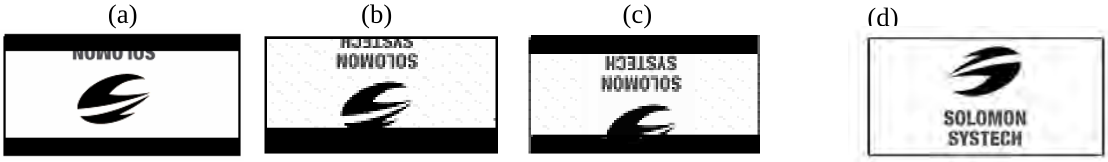
(RAM)

Table 10-2: Example of Set Display Offset and Display Start Line with Remap

Hardware pin name	Output														
	64		64		64		48		48		48		48		Set MUX ration (A8h)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap		COM normal / remap (C0h / C8h)
	0		8		0		0		8		0		8		Display offset (D3h)
	0		0		8		0		0		8		16		Display start line (40h - 7Fh)
COM0	ROW63	RAM63	ROW7	RAM7	ROW63	RAM7	ROW47	RAM47	-	-	ROW47	RAM55	-	-	
COM1	ROW62	RAM62	ROW6	RAM6	ROW62	RAM6	ROW46	RAM46	-	-	ROW46	RAM54	-	-	
COM2	ROW61	RAM61	ROW5	RAM5	ROW61	RAM5	ROW45	RAM45	-	-	ROW45	RAM53	-	-	
COM3	ROW60	RAM60	ROW4	RAM4	ROW60	RAM4	ROW44	RAM44	-	-	ROW44	RAM52	-	-	
COM4	ROW59	RAM59	ROW3	RAM3	ROW59	RAM3	ROW43	RAM43	-	-	ROW43	RAM51	-	-	
COM5	ROW58	RAM58	ROW2	RAM2	ROW58	RAM2	ROW42	RAM42	-	-	ROW42	RAM50	-	-	
COM6	ROW57	RAM57	ROW1	RAM1	ROW57	RAM1	ROW41	RAM41	-	-	ROW41	RAM49	-	-	
COM7	ROW56	RAM56	ROW0	RAM0	ROW56	RAM0	ROW40	RAM40	-	-	ROW40	RAM48	-	-	
COM8	ROW55	RAM55	ROW63	RAM63	ROW55	RAM63	ROW39	RAM39	ROW47	RAM47	ROW39	RAM47	ROW47	RAM63	
COM9	ROW54	RAM54	ROW62	RAM62	ROW54	RAM62	ROW38	RAM38	ROW46	RAM46	ROW38	RAM46	ROW46	RAM62	
COM10	ROW53	RAM53	ROW61	RAM61	ROW53	RAM61	ROW37	RAM37	ROW45	RAM45	ROW37	RAM45	ROW45	RAM61	
COM11	ROW52	RAM52	ROW60	RAM60	ROW52	RAM60	ROW36	RAM36	ROW44	RAM44	ROW36	RAM44	ROW44	RAM60	
COM12	ROW51	RAM51	ROW59	RAM59	ROW51	RAM59	ROW35	RAM35	ROW43	RAM43	ROW35	RAM43	ROW43	RAM59	
COM13	ROW50	RAM50	ROW58	RAM58	ROW50	RAM58	ROW34	RAM34	ROW42	RAM42	ROW34	RAM42	ROW42	RAM58	
COM14	ROW49	RAM49	ROW57	RAM57	ROW49	RAM57	ROW33	RAM33	ROW41	RAM41	ROW33	RAM41	ROW41	RAM57	
COM15	ROW48	RAM48	ROW56	RAM56	ROW48	RAM56	ROW32	RAM32	ROW40	RAM40	ROW32	RAM40	ROW40	RAM56	
COM16	ROW47	RAM47	ROW55	RAM55	ROW47	RAM55	ROW31	RAM31	ROW39	RAM39	ROW31	RAM39	ROW39	RAM55	
COM17	ROW46	RAM46	ROW54	RAM54	ROW46	RAM54	ROW30	RAM30	ROW38	RAM38	ROW30	RAM38	ROW38	RAM54	
COM18	ROW45	RAM45	ROW53	RAM53	ROW45	RAM53	ROW29	RAM29	ROW37	RAM37	ROW29	RAM37	ROW37	RAM53	
COM19	ROW44	RAM44	ROW52	RAM52	ROW44	RAM52	ROW28	RAM28	ROW36	RAM36	ROW28	RAM36	ROW36	RAM52	
COM20	ROW43	RAM43	ROW51	RAM51	ROW43	RAM51	ROW27	RAM27	ROW35	RAM35	ROW27	RAM35	ROW35	RAM51	
COM21	ROW42	RAM42	ROW50	RAM50	ROW42	RAM50	ROW26	RAM26	ROW34	RAM34	ROW26	RAM34	ROW34	RAM50	
COM22	ROW41	RAM41	ROW49	RAM49	ROW41	RAM49	ROW25	RAM25	ROW33	RAM33	ROW25	RAM33	ROW33	RAM49	
COM23	ROW40	RAM40	ROW48	RAM48	ROW40	RAM48	ROW24	RAM24	ROW32	RAM32	ROW24	RAM32	ROW32	RAM48	
COM24	ROW39	RAM39	ROW47	RAM47	ROW39	RAM47	ROW23	RAM23	ROW31	RAM31	ROW23	RAM31	ROW31	RAM47	
COM25	ROW38	RAM38	ROW46	RAM46	ROW38	RAM46	ROW22	RAM22	ROW30	RAM30	ROW22	RAM30	ROW30	RAM46	
COM26	ROW37	RAM37	ROW45	RAM45	ROW37	RAM45	ROW21	RAM21	ROW29	RAM29	ROW21	RAM29	ROW29	RAM45	
COM27	ROW36	RAM36	ROW44	RAM44	ROW36	RAM44	ROW20	RAM20	ROW28	RAM28	ROW20	RAM28	ROW28	RAM44	
COM28	ROW35	RAM35	ROW43	RAM43	ROW35	RAM43	ROW19	RAM19	ROW27	RAM27	ROW19	RAM27	ROW27	RAM43	
COM29	ROW34	RAM34	ROW42	RAM42	ROW34	RAM42	ROW18	RAM18	ROW26	RAM26	ROW18	RAM26	ROW26	RAM42	
COM30	ROW33	RAM33	ROW41	RAM41	ROW33	RAM41	ROW17	RAM17	ROW25	RAM25	ROW17	RAM25	ROW25	RAM41	
COM31	ROW32	RAM32	ROW40	RAM40	ROW32	RAM40	ROW16	RAM16	ROW24	RAM24	ROW16	RAM24	ROW24	RAM40	
COM32	ROW31	RAM31	ROW39	RAM39	ROW31	RAM39	ROW15	RAM15	ROW23	RAM23	ROW15	RAM23	ROW23	RAM39	
COM33	ROW30	RAM30	ROW38	RAM38	ROW30	RAM38	ROW14	RAM14	ROW22	RAM22	ROW14	RAM22	ROW22	RAM38	
COM34	ROW29	RAM29	ROW37	RAM37	ROW29	RAM37	ROW13	RAM13	ROW21	RAM21	ROW13	RAM21	ROW21	RAM37	
COM35	ROW28	RAM28	ROW36	RAM36	ROW28	RAM36	ROW12	RAM12	ROW20	RAM20	ROW12	RAM20	ROW20	RAM36	
COM36	ROW27	RAM27	ROW35	RAM35	ROW27	RAM35	ROW11	RAM11	ROW19	RAM19	ROW11	RAM19	ROW19	RAM35	
COM37	ROW26	RAM26	ROW34	RAM34	ROW26	RAM34	ROW10	RAM10	ROW18	RAM18	ROW10	RAM18	ROW18	RAM34	
COM38	ROW25	RAM25	ROW33	RAM33	ROW25	RAM33	ROW9	RAM9	ROW17	RAM17	ROW9	RAM17	ROW17	RAM33	
COM39	ROW24	RAM24	ROW32	RAM32	ROW24	RAM32	ROW8	RAM8	ROW16	RAM16	ROW8	RAM16	ROW16	RAM32	
COM40	ROW23	RAM23	ROW31	RAM31	ROW23	RAM31	ROW7	RAM7	ROW15	RAM15	ROW7	RAM15	ROW15	RAM31	
COM41	ROW22	RAM22	ROW30	RAM30	ROW22	RAM30	ROW6	RAM6	ROW14	RAM14	ROW6	RAM14	ROW14	RAM30	
COM42	ROW21	RAM21	ROW29	RAM29	ROW21	RAM29	ROW5	RAM5	ROW13	RAM13	ROW5	RAM13	ROW13	RAM29	
COM43	ROW20	RAM20	ROW28	RAM28	ROW20	RAM28	ROW4	RAM4	ROW12	RAM12	ROW4	RAM12	ROW12	RAM28	
COM44	ROW19	RAM19	ROW27	RAM27	ROW19	RAM27	ROW3	RAM3	ROW11	RAM11	ROW3	RAM11	ROW11	RAM27	
COM45	ROW18	RAM18	ROW26	RAM26	ROW18	RAM26	ROW2	RAM2	ROW10	RAM10	ROW2	RAM10	ROW10	RAM26	
COM46	ROW17	RAM17	ROW25	RAM25	ROW17	RAM25	ROW1	RAM1	ROW9	RAM9	ROW1	RAM9	ROW9	RAM25	
COM47	ROW16	RAM16	ROW24	RAM24	ROW16	RAM24	ROW0	RAM0	ROW8	RAM8	ROW0	RAM8	ROW8	RAM24	
COM48	ROW15	RAM15	ROW23	RAM23	ROW15	RAM23	-	-	ROW7	RAM7	-	-	ROW7	RAM23	
COM49	ROW14	RAM14	ROW22	RAM22	ROW14	RAM22	-	-	ROW6	RAM6	-	-	ROW6	RAM22	
COM50	ROW13	RAM13	ROW21	RAM21	ROW13	RAM21	-	-	ROW5	RAM5	-	-	ROW5	RAM21	
COM51	ROW12	RAM12	ROW20	RAM20	ROW12	RAM20	-	-	ROW4	RAM4	-	-	ROW4	RAM20	
COM52	ROW11	RAM11	ROW19	RAM19	ROW11	RAM19	-	-	ROW3	RAM3	-	-	ROW3	RAM19	
COM53	ROW10	RAM10	ROW18	RAM18	ROW10	RAM18	-	-	ROW2	RAM2	-	-	ROW2	RAM18	
COM54	ROW9	RAM9	ROW17	RAM17	ROW9	RAM17	-	-	ROW1	RAM1	-	-	ROW1	RAM17	
COM55	ROW8	RAM8	ROW16	RAM16	ROW8	RAM16	-	-	ROW0	RAM0	-	-	ROW0	RAM16	
COM56	ROW7	RAM7	ROW15	RAM15	ROW7	RAM15	-	-	-	-	-	-	-	-	
COM57	ROW6	RAM6	ROW14	RAM14	ROW6	RAM14	-	-	-	-	-	-	-	-	
COM58	ROW5	RAM5	ROW13	RAM13	ROW5	RAM13	-	-	-	-	-	-	-	-	
COM59	ROW4	RAM4	ROW12	RAM12	ROW4	RAM12	-	-	-	-	-	-	-	-	
COM60	ROW3	RAM3	ROW11	RAM11	ROW3	RAM11	-	-	-	-	-	-	-	-	
COM61	ROW2	RAM2	ROW10	RAM10	ROW2	RAM10	-	-	-	-	-	-	-	-	
COM62	ROW1	RAM1	ROW9	RAM9	ROW1	RAM9	-	-	-	-	-	-	-	-	
COM63	ROW0	RAM0	ROW8	RAM8	ROW0	RAM8	-	-	-	-	-	-	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		(g)		



(a) (b) (c) (d)



(e) (f) (g) (RAM)

10.16 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D) (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 0000b. Please refer to section 8.3 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 1000b.

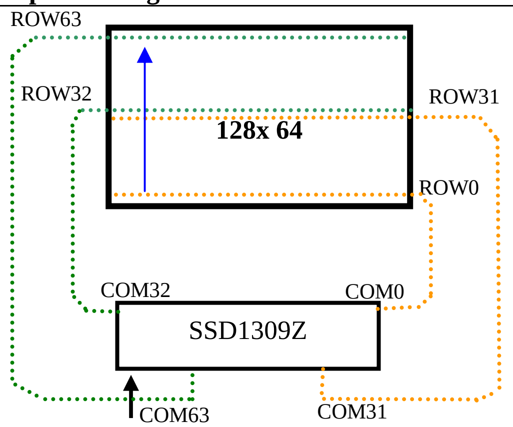
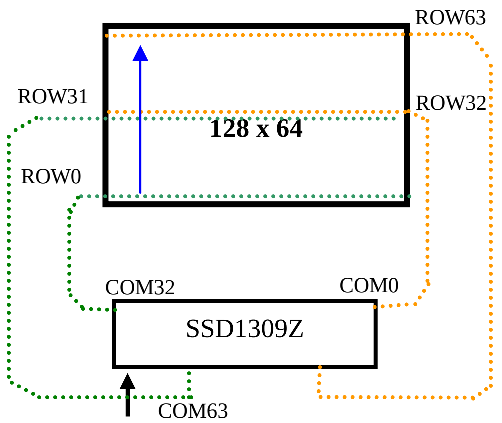
10.17 Set Pre-charge Period (D9h)

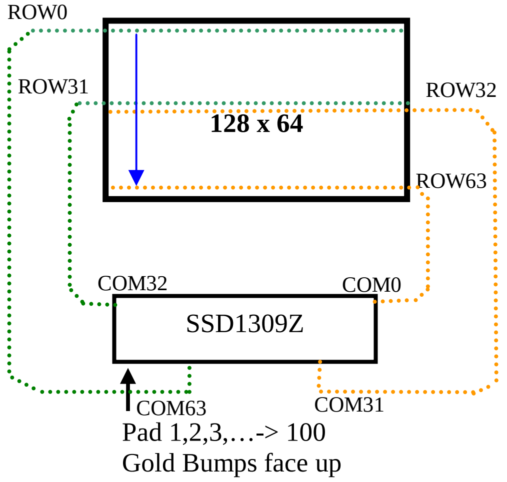
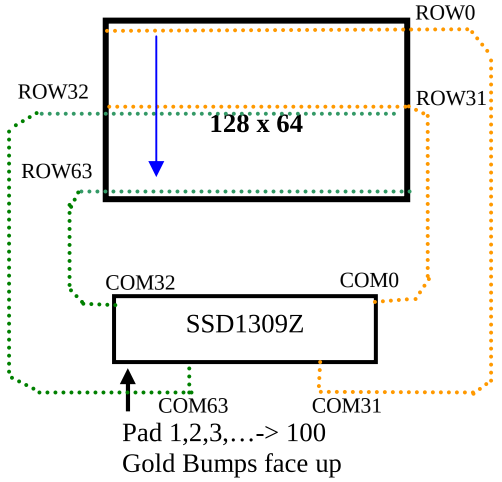
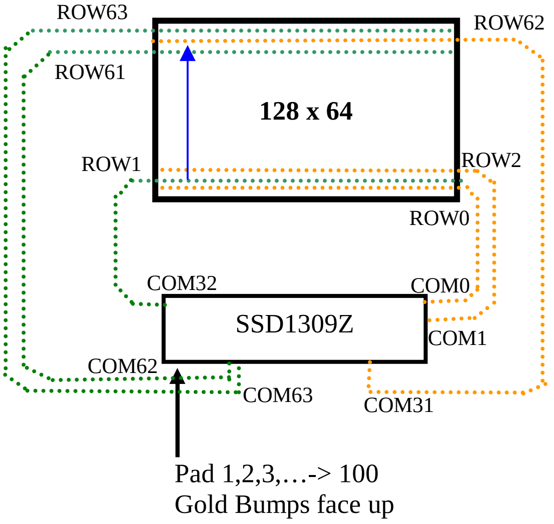
This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals to 2 DCLKs.

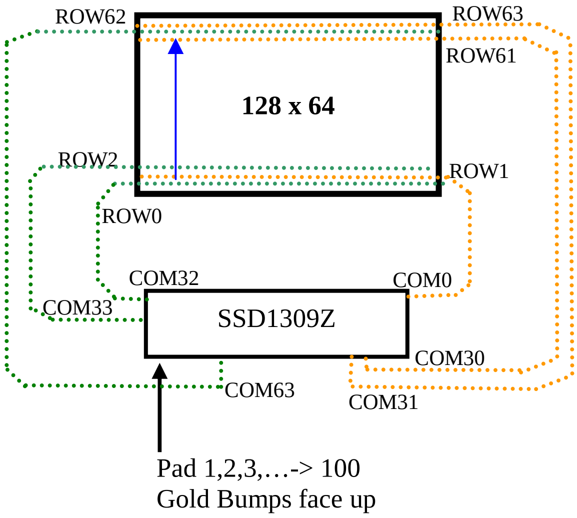
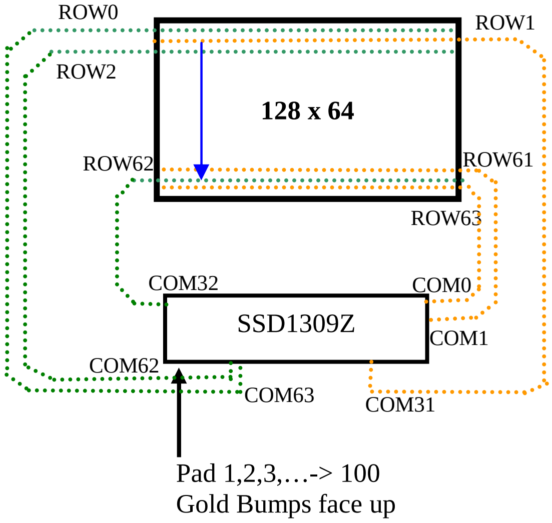
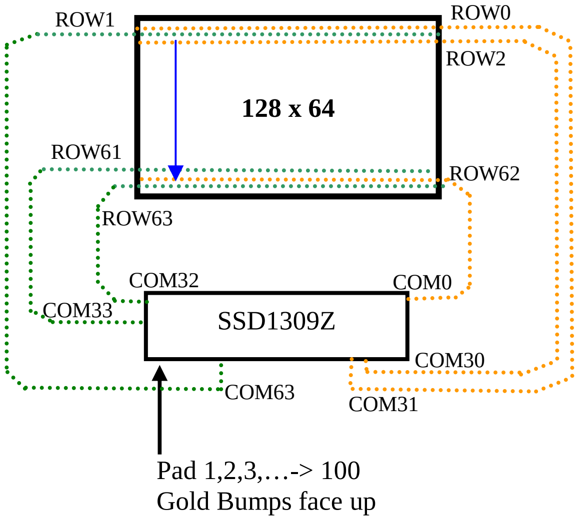
10.18 Set COM Pins Hardware Configuration (DAh)

This command sets the COM signals pin configuration to match the OLED panel hardware layout. The table below shows the COM pin configuration under different conditions (for MUX ratio =64):

Table 10-3 : COM Pins Hardware Configuration

Conditions	COM pins Configurations
1 Sequential COM pin configuration (DAh A[4] =0) COM output Scan direction: from COM0 to COM63 (C0h) Disable COM Left/Right remap (DAh A[5] =0)	 Pad 1,2,3,…->100 Gold Bumps face up
2 Sequential COM pin configuration (DAh A[4] =0) COM output Scan direction: from COM0 to COM63 (C0h) Enable COM Left/Right remap (DAh A[5] =1)	 Pad 1,2,3,…-> 100 Gold Bumps face up

<table>
<tr><th>Conditions</th><th>COM pins Configurations</th></tr>
<tr><td>3 Sequential COM pin configuration (DAh A[4] =0)
COM output Scan direction: from COM63 to COM0 (C8h)
Disable COM Left/Right remap (DAh A[5] =0)</td><td>
</td></tr>
<tr><td>4 Sequential COM pin configuration (DAh A[4] =0)
COM output Scan direction: from COM63 to COM0 (C8h)
Enable COM Left/Right remap (DAh A[5] =1)</td><td>
</td></tr>
<tr><td>5 Alternative COM pin configuration (DAh A[4] =1)
COM output Scan direction: from COM0 to COM63 (C0h)
Disable COM Left/Right remap (DAh A[5] =0)</td><td>
</td></tr>
</table>

Conditions	COM pins Configurations
6 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM0 to COM63 (C0h) Enable COM Left/Right remap (DAh A[5] =1)	
7 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM63 to COM0(C8h) Disable COM Left/Right remap (DAh A[5] =0)	
8 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM63 to COM0(C8h) Enable COM Left/Right remap (DAh A[5] =1)	

10.19 Set V_{COMH} Deselect Level (DBh)

This command adjusts the V_{COMH} regulator output.

10.20 Set GPIO (DCh)

This double byte command is used to set the state of GPIO pin. Refer to Table 9-4 for details.

10.21 NOP (E3h)

No Operation Command.

10.22 Set Command Lock (FDh)

This double byte command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is called "Lock" state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the "Lock" state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resumes from the "Lock" state, and the driver IC will then respond to the command and memory access.

10.23 Horizontal Scroll Setup (26h/27h)

This command consists of seven consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start page, end page, scrolling speed, start column and end column; refer to Table 9-2 for details.

Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

The SSD1309 horizontal scroll is designed for 128 columns scrolling. The following two figures (Figure 10-7, Figure 10-8, and Figure 10-9) show the examples of using the horizontal scroll:

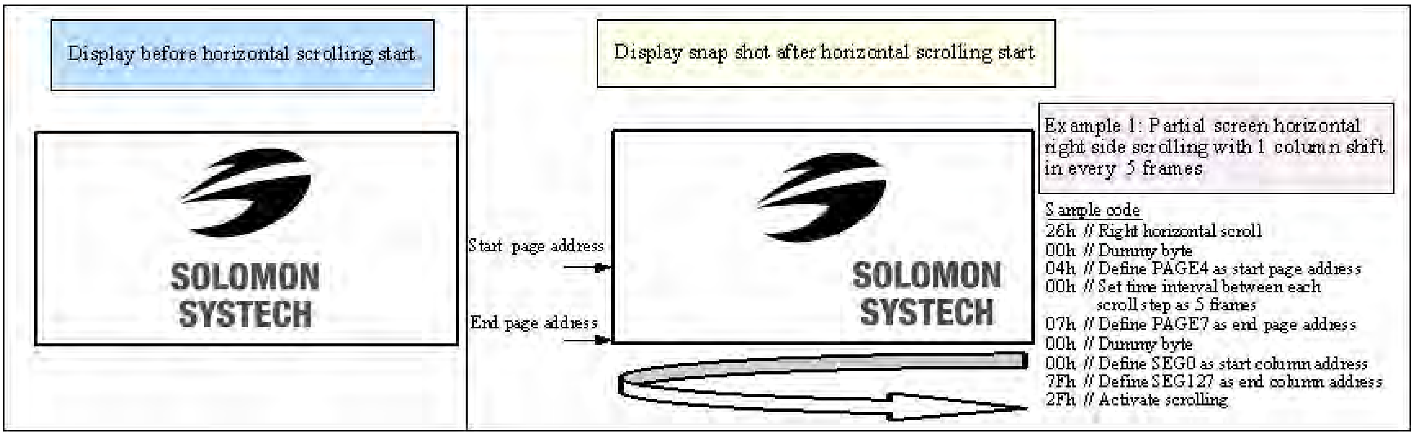
Figure 10-7: Horizontal scroll example: Scroll RIGHT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	…	…	…	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
After one scroll step	SEG127	SEG0	SEG1	SEG2	SEG3	SEG4	…	…	…	SEG121	SEG122	SEG123	SEG124	SEG125	SEG126

Figure 10-8: Horizontal scroll example: Scroll LEFT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	⋮	⋮	⋮	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
After one scroll step	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	⋮	⋮	⋮	SEG123	SEG124	SEG125	SEG126	SEG127	SEG0

Figure 10-9: Horizontal scrolling setup example (LS pin pull LOW)



10.24 Continuous Vertical and Horizontal Scroll Setup (29h/2Ah)

This command consists of seven consecutive bytes to set up the continuous vertical scroll parameters and determine the scrolling start page, end page, scrolling speed and vertical scrolling offset; refer to Table 9-2 for details.

If the vertical scrolling offset byte E[5:0] of command 29h / 2Ah is set to zero, then only horizontal scrolling is performed (like command 26/27h). On the other hand, if the number of column scroll offset byte A[0] is set to zero, then only vertical scrolling is performed.

Continuous diagonal (horizontal + vertical) scrolling would be enabled if both A[0] and E[5:0] are set to be non-zero, whereas full column diagonal scrolling mode is suggested by setting F[7:0]=00h and G[7:0]=7Fh.

Before issuing this command the scroll must be deactivated (2Eh), or otherwise, RAM content may be corrupted. The following figures (Figure 10-10 and Figure 10-11) show the examples of using the continuous vertical scroll and the continuous diagonal scroll, respectively.

Figure 10-10: Continuous Vertical scrolling setup example (LS pin pull LOW)

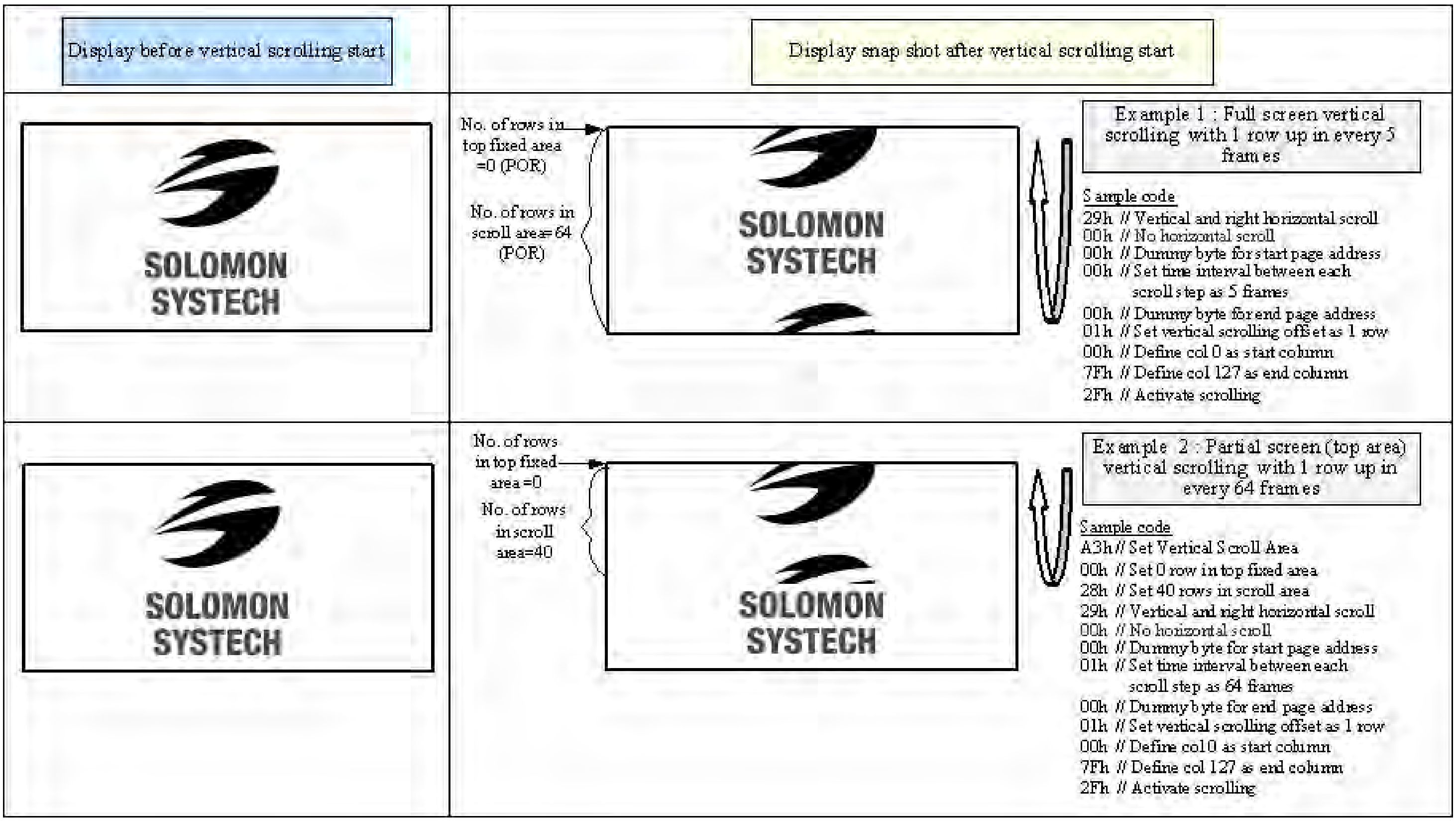
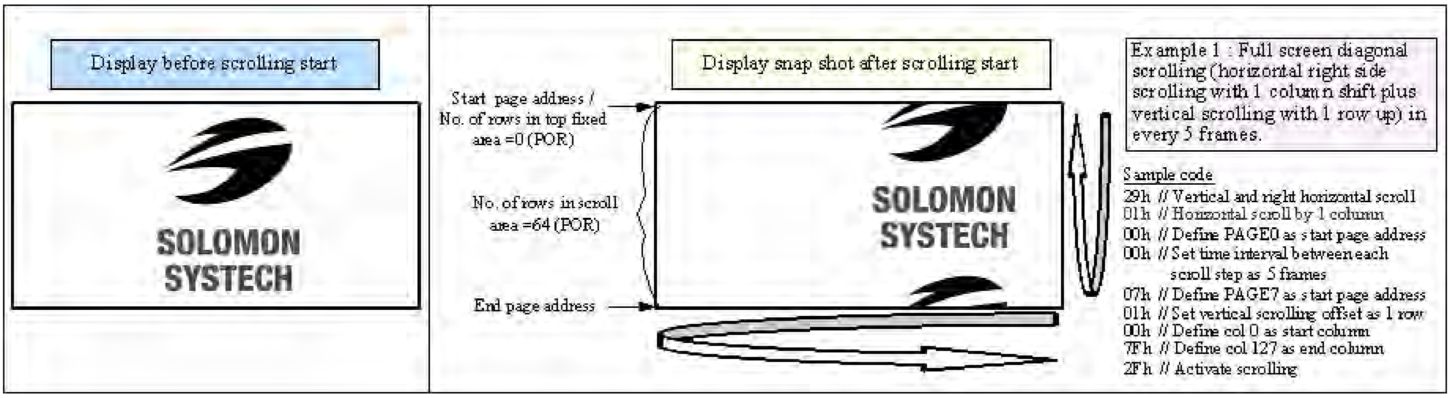


Figure 10-11: Continuous Vertical and Horizontal scrolling setup example (LS pin pull LOW)



10.25 Deactivate Scroll (2Eh)

This command stops the motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

10.26 Activate Scroll (2Fh)

This command starts the motion of scrolling and should only be issued after the scroll setup parameters have been defined by the scrolling setup commands: 26h / 27h / 29h / 2Ah. The setting in the latest scrolling setup command overwrites the setting in the previous scrolling setup command.

The following actions are prohibited after the scrolling is activated

1. RAM access (Data write or read)
2. Changing the horizontal scroll setup parameters

10.27 Set Vertical Scroll Area (A3h)

This command consists of 3 consecutive bytes to set up the vertical scroll area. For the continuous vertical scroll function (command 29h / 2Ah), the number of rows in the vertical scroll area can be set smaller than or equating to the MUX ratio. Figure 10-10 shows a vertical scrolling example with different settings in vertical scroll area.

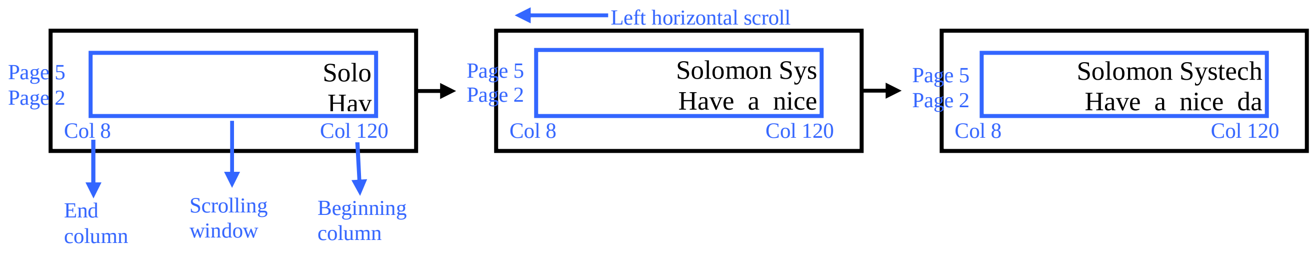
10.28 Content Scroll Setup (2Ch/2Dh)

This command consists of seven consecutive bytes to set up the horizontal scroll parameters and determine the scrolling start page, end page, start column and end column. One column will be scrolled horizontally by sending the setting of command 2Ch / 2Dh once.

When command 2Ch / 2Dh are sent consecutively, a delay time of $2/FrameFreq$ must be set.

Figure 10-12 shown an example of using 2Dh “Content Scroll Setup” command for horizontal scrolling to left with infinite content update. In there, “Col” means the graphic display data RAM column.

Figure 10-12: Content Scrolling example (2Dh, Left Horizontal Scroll by one column)



By using command 2Ch/2Dh, RAM contents are scrolled and updated by one column. Table 10-4 is an example of content scrolling setting of SSD1309 (scrolling window of 4 pages). The values of registers depend on different conditions and applications.

Table 10-4 : Content Scrolling software flow example (Page addressing mode – command 20h, 02h)

Step	Action	D/C#	Code	Remarks
1	**For i= 1 to n**	-	-	Create "For loop" for infinite content scrolling
2	Set Content scrolling command (scrolling window : Page 2 to 5, Col 8 to Col 120)	0	2Dh	Left Horizontal Scroll by one column
		0	00h	A[7:0] : Dummy byte (Set as 00h)
		0	02h	B[2:0] : Define start page address
		0	01h	C[7:0] : Dummy byte (Set as 01h)
		0	05h	D[2:0] : Define end page address
		0	00h	E[7:0] : Dummy byte (Set as 00h)
		0	08h	F[6:0] : Define start column address
		0	78h	G[6:0] : Define end column address
3	Add Delay time of $2/FrameFreq$	-	-	E.g. Delay 20ms if frame freq ≈ 100Hz
4	Write RAM on the beginning column of the scrolling window			
	Write RAM on (Page2, Col 120) *(Content update in beginning column)*	0	B2h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
	Write RAM on (Page3, Col 120) *(Content update in beginning column)*	0	B3h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
	Write RAM on (Page4, Col 120) *(Content update in beginning column)*	0	B4h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
	Write RAM on (Page5, Col 120) *(Content update in beginning column)*	0	B5h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
5	i=i+1	-	-	Go to next "For loop"
	Delay timing	-	-	Set time interval between each scroll step if necessary
	End			

There are 3 different memory addressing mode in SSD1309: page addressing mode, horizontal addressing mode and vertical addressing mode and it is selected by command 20h. Table 10-4 is an example of content scrolling software flow under page addressing mode, while vertical addressing mode example is shown in below Table 10-5.

Table 10-5 : Content Scrolling setting example (Vertical addressing mode – command 20h, 01h)

Step	**Action**	**D/C#**	**Code**	**Remarks**
1	**For i= 1 to n**	-	-	Create "For loop" for infinite content scrolling
2	Set Content scrolling command (scrolling window : Page 2 to 5, Col 8 to Col 120)	0	2Dh	Left Horizontal Scroll by one column
		0	00h	A[7:0] : Dummy byte (Set as 00h)
		0	02h	B[2:0] : Define start page address
		0	01h	C[7:0] : Dummy byte (Set as 01h)
		0	05h	D[2:0] : Define end page address
		0	00h	E[7:0] : Dummy byte (Set as 00h)
		0	08h	F[6:0] : Define start column address
		0	78h	G[6:0] : Define end column address
3	Add Delay time of $2/FrameFreq$	-	-	E.g. Delay 20ms if frame freq ≈ 100Hz
4	Write RAM on the beginning column of the scrolling window (Page 2 to 5, Col 120) *(Content update in beginning column)*	0	21h	Set Column address
		0	78h	Set column start address for Vertical Addressing Mode
		0	78h	Set column end address for Vertical Addressing Mode
		0	22h	Set Page address
		0	02h	Set start page address for Vertical Addressing Mode
		0	05h	Set end page address for Vertical Addressing Mode
		1	-	Write data to fill the RAM
5	i=i+1	-	-	Go to next "For loop"
	Delay timing	-	-	Set time interval between each scroll step if necessary
	End			

11 MAXIMUM RATINGS

Table 11-1 : Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{CC}		0 to 17	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS}, V_{DD} =1.65 V to 3.3V, T_A = 25°C

Table 12-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	7	-	16	V
V_{DD}	Logic Supply Voltage	-	1.65	-	3.3	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9 x V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1 x V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8 x V_{DD}	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2 x V_{DD}	V
$I_{DD,SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~16V Display OFF, No panel attached	-	-	10	uA
$I_{CC,SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~16V Display OFF, No panel attached	-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DD} = 2.8V, V_{CC} =12, I_{REF} =10uA, No loading, Display ON, All ON	Contrast = FFh	-	450	580	uA
I_{DD}	V_{DD} Supply Current V_{DD} =2.8V, V_{CC} = 12, I_{REF} = 10uA , No loading, Display ON, All ON,		-	90	110	uA
I_{SEG}	Segment Output Current, V_{DD} = 2.8V, V_{CC}=12V, I_{REF}=10uA, Display ON.	Contrast=FFh	280	310	340	uA
		Contrast=AFh	-	215	-	
		Contrast=7Fh	-	155	-	
		Contrast=3Fh	-	78	-	
		Contrast=0Fh	-	20	-	
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:127] = Segment current at contrast setting = FFh	-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast setting = FFh)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%

13 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD}=1.65 to3.3V
T_A = 25°C

Table 13-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.8V	360	450	540	kHz
F_{FRM}	Frame Frequency	128x64 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} x 1/(DxKx64) (2)	-	Hz
RES#	Reset low pulse width		3	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command D5h A[7:4] is in default value.

(2) D: divide ratio (default value = 1)
K: number of display clocks per row period (default value = 69)
Please refer to 9.5 (Set Display Clock Divide Ratio/Oscillator Frequency, D5h) for detailed description

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	20	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DW}	Data Write Time	80	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-1 : 6800-series MCU parallel interface characteristics

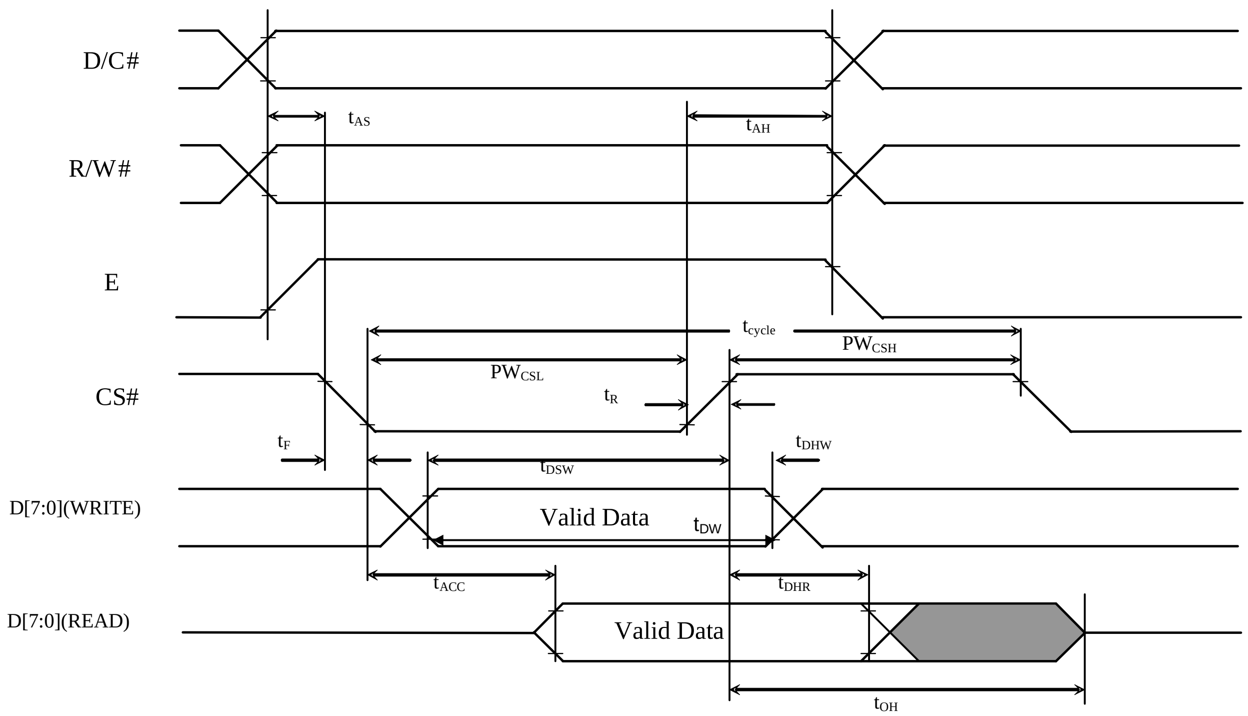


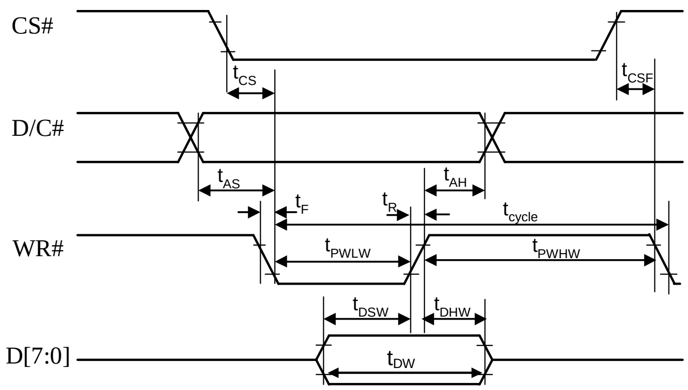
Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V ~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	20	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DW}	Data Write Time	70	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series parallel interface characteristics

Write cycle



Read Cycle

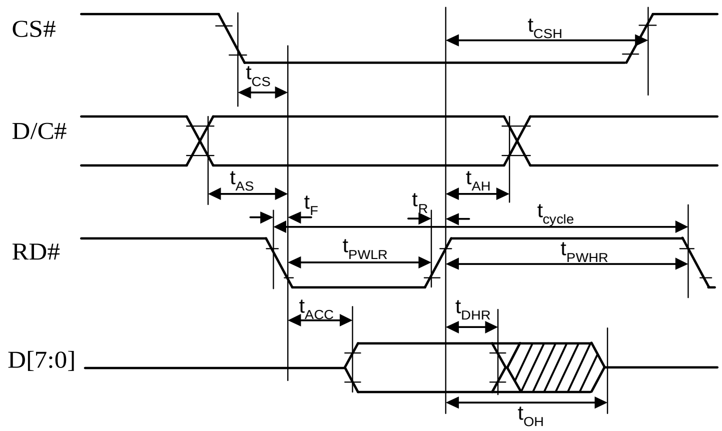
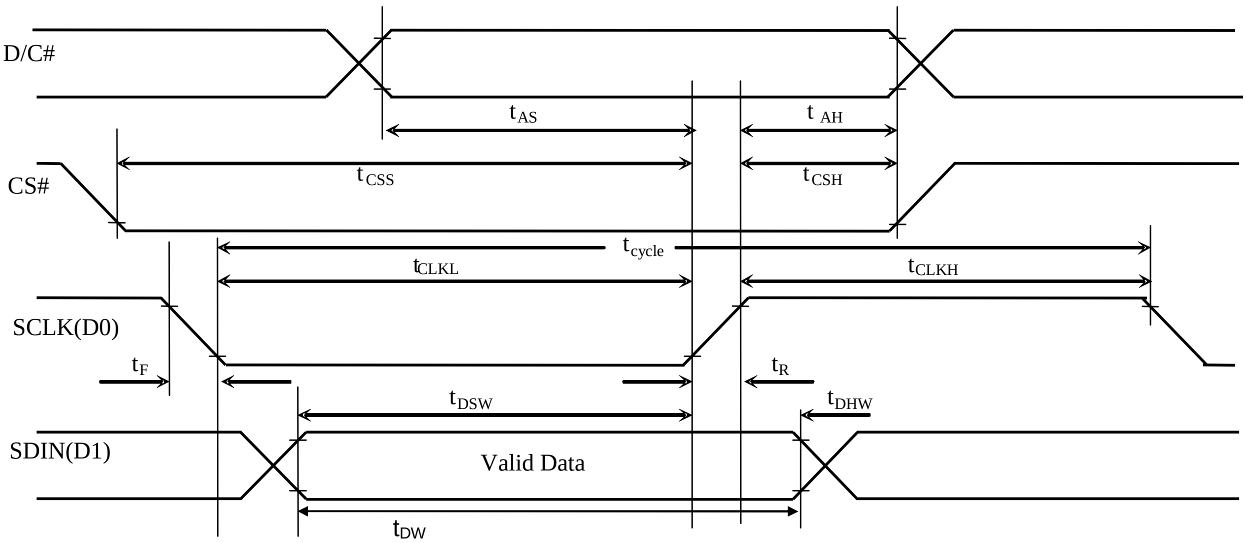


Table 13-4 : Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	50	-	-	ns
t_{DW}	Data Write Time	55	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	50	-	-	ns
t_{CLKH}	Clock High Time	50	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-3 : Serial interface characteristics (4-wire SPI)



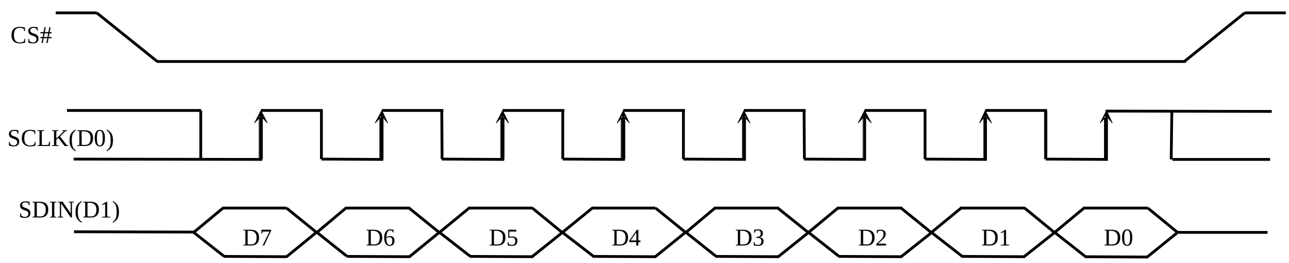
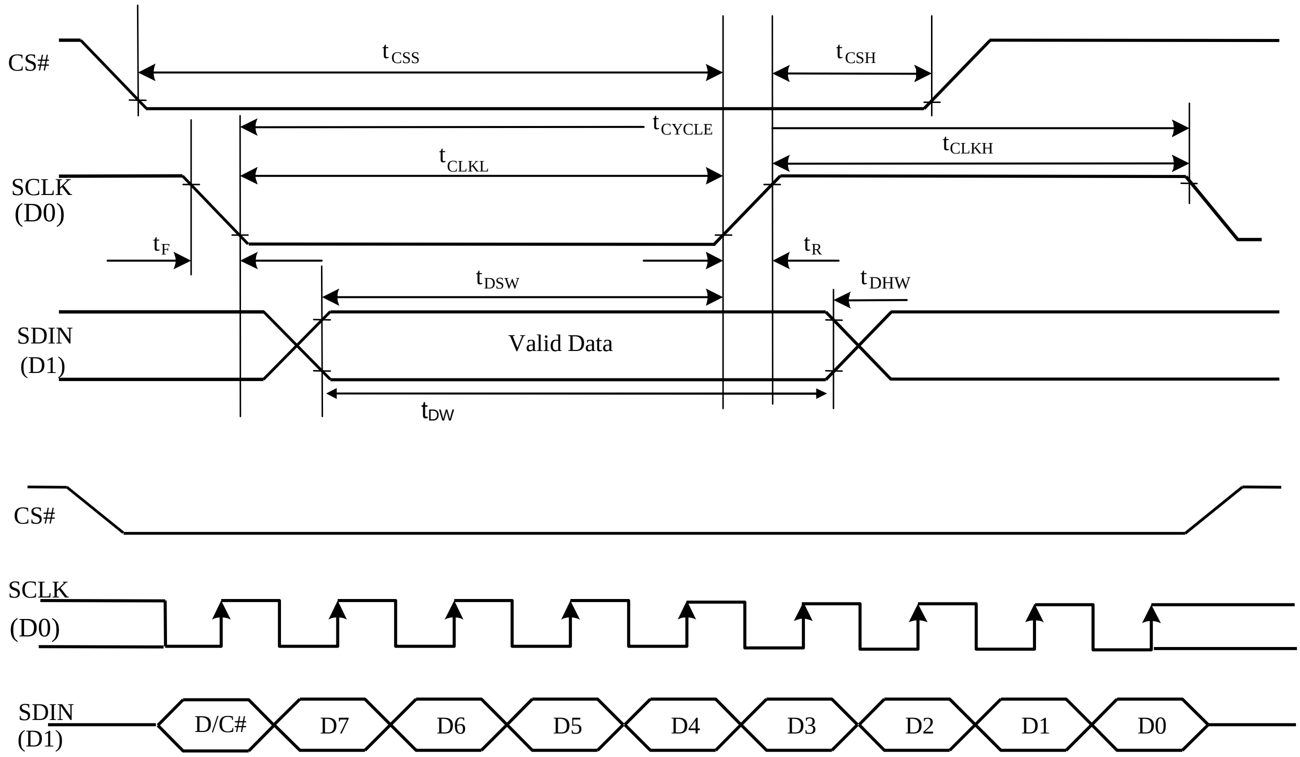


Table 13-5 : Serial Interface Timing Characteristics (3-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	50	-	-	ns
t_{DW}	Data Write Time	55	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	50	-	-	ns
t_{CLKH}	Clock High Time	50	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-4 : Serial interface characteristics (3-wire SPI)



Conditions:

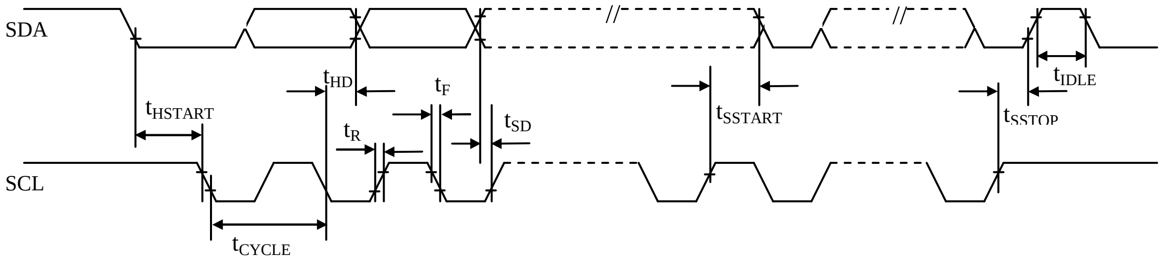
V_{DD} - V_{SS} = 1.65V ~ 3.3V

T_A = 25°C

Table 13-6 : I²C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

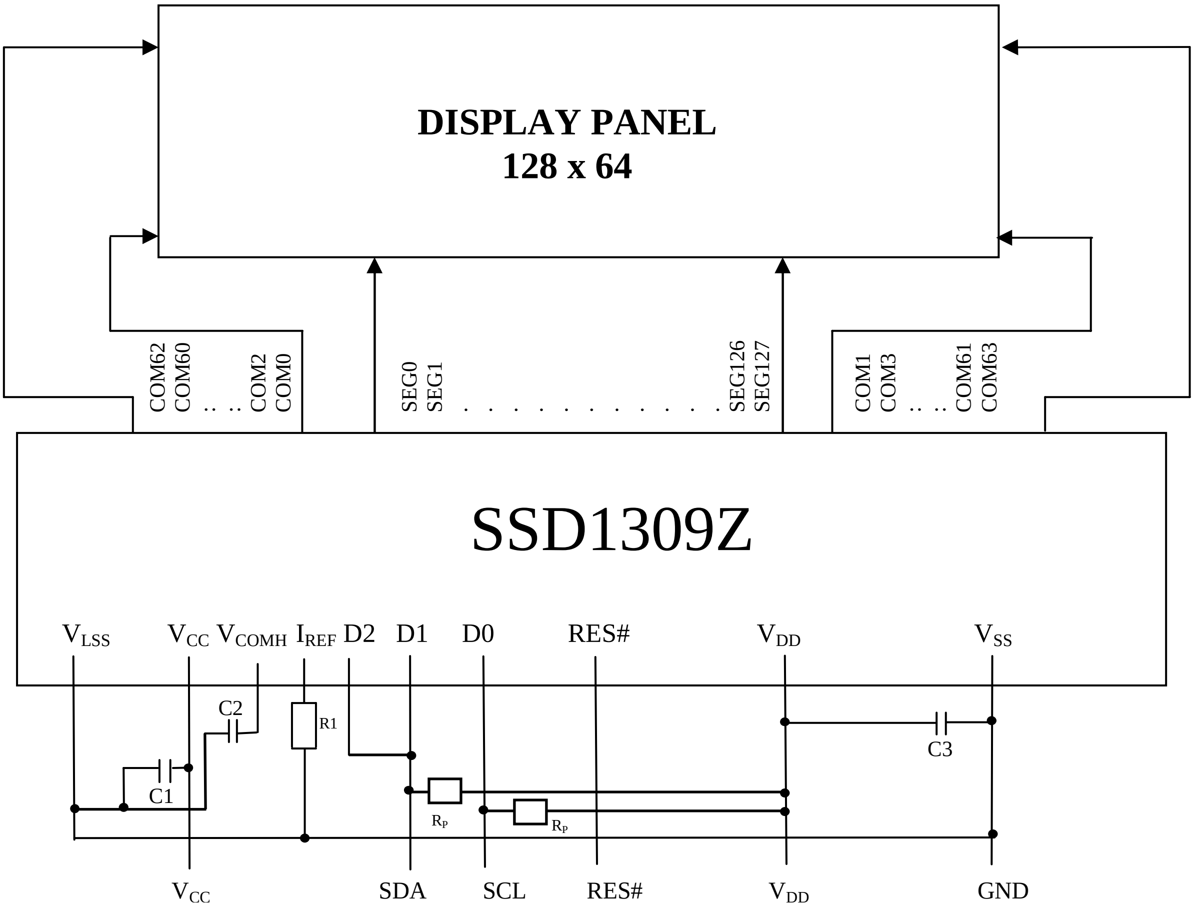
Figure 13-5 : I²C interface Timing characteristics



14 Application Example

Figure 14-1 : Application Example of SSD1309Z

The configuration for I^2C interface mode is shown in the following diagram:
(V_{DD}=2.8V, V_{CC} =12V, I_{REF}=10uA)



Pin connected to MCU interface: D[2:0], RES#
Pin internally connected to V_{SS}: D[7:3], BS0, BS2, E, R/W#, CS#, CL, V_{SS1}
Pin internally connected to V_{DD}: BS1, CLS
TR[7:0] should be left open.
D/C# acts as SA0 for slave address selection (3)

C1, C2: 2.2uF (1)
C3: 1.0uF (1) place close to IC V_{DD} and V_{SS} pins on PCB
R_P : Pull up resistor

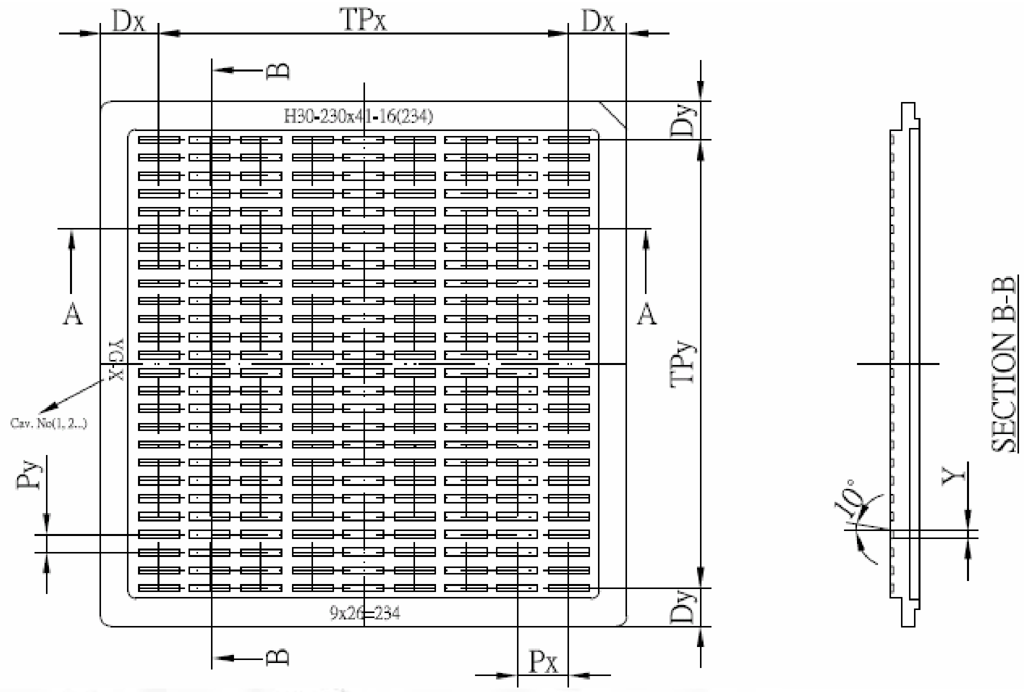
Voltage at I_{REF} = V_{CC} – 3V. For V_{CC} = 12V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
≈ (12-3)V / 10uA
= 900KΩ

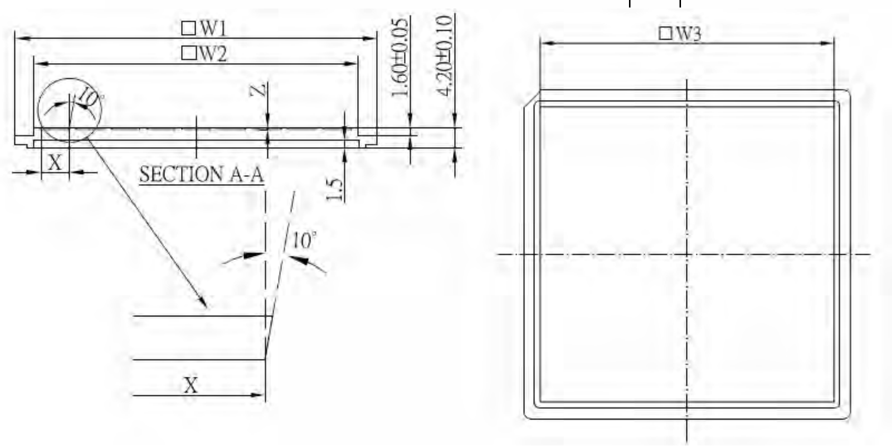
Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) Die gold bump face down.
(3) Refer to Section 8.1.5 for details.
(4) It is recommended to tie V_{LSS} and V_{SS} at one common ground point to minimize circulating ground noise.

15 PACKAGE INFORMATION

15.1 SSD1309Z Die Tray Information

Figure 15-1: SSD1309Z die tray information





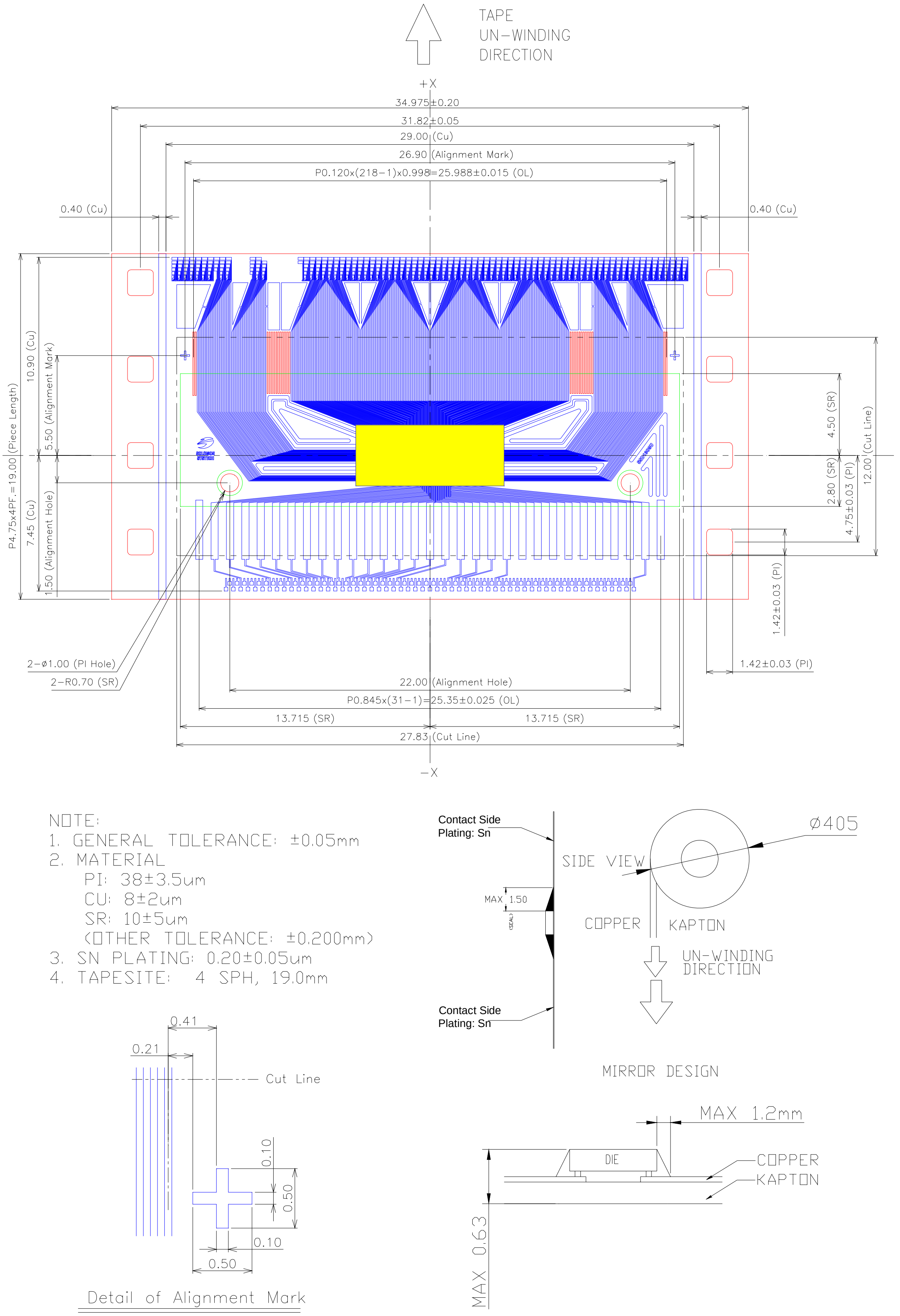
Remarks:

1. Tray material: Permanent Antistatic
2. Tray color code: Black
3. Surface resistance 10^9 ~ 10^{12} Ω
4. Pocket bottom: Rough Surface

Parameter	Dimensions
	mm (mil)
W1	76.00±0.10 (2992)
W2	68.00±0.10 (2677)
W3	68.30±0.10 (2689)
D_X	8.40±0.10 (331)
TP_X	59.20±0.10 (2331)
D_Y	5.50±0.10 (217)
TP_Y	65.00±0.10 (2559)
P_X	7.40±0.05 (291)
P_Y	2.60±0.05 (102)
X	5.85±0.05 (230)
Y	1.02±0.05 (41)
Z	0.40±0.05 (16)
N (pocket number)	234

15.2 SSD1309UR1 Detail Dimension

Figure 15-2 SSD1309UR1 Detail Dimension



The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People's Republic of China Electronic Industry Standard SJ/T 11363-2006 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)". Hazardous Substances test report is available upon request.

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